SHANGHAI SINO-IC MICROELECTRONICS CO., LTD.

Jul 2015

SE6003

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

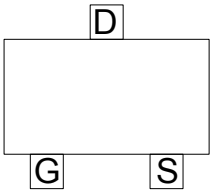
Features

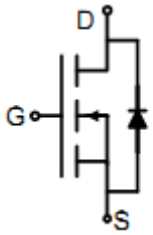
For a single MOSFET

- V_{DS} = 65V
- $R_{DS(ON)}$ = 62mΩ @ V_{GS}=10V
- $R_{DS(ON)}$ = 88mΩ @ V_{GS}=4.5V

Pin configurations

See Diagram below





Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	65	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	3	A
	Pulsed		12	
Total Power Dissipation	@TA=25℃	P_D	1.38	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Junction to Ambient (t≦10s)	-	90	℃/W

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	65			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= 48V, V_{GS}=0V			25	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20 V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1	1.7	3.0	V
g_{fs}	Forward Transconductance	V_{DS}= 10V, I_D=3A		7		S
$R_{DS(ON)}$	Static Drain-Source On-Resistance [2]	V_{GS}=10V, I_D=3A		62	80	mΩ
		V_{GS}=4.5V, I_D=2A		88	120	
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		460	740	pF
C_{oss}	Output Capacitance			35		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=30V, I_D=3A		6	9.6	nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=30V, R_{GEN}=3.3Ω I_D=1A		5		ns
$t_{d(off)}$	Turn-Off Delay Time			17		ns
$t_{d(r)}$	Turn-On Rise Time			6		ns
$t_{d(f)}$	Turn-Off Fall Time			3.5		ns
Source-Drain Diode						
Symbol	**Parameter**	Test Condition	**Min**	**Typ**	**Max**	**Units**
V_{SD}	Forward On voltage[2]	I_S=1A，V_{GS}=0V			1.3	V
t_{rr}	Reverse Recovery Time	IS=3A,VGS=0V dI/dt=100A/		21		ns
Q_{rr}	Reverse Recovery Charge			19		nC

Note 1: Pulse width limited by Max. junction temperature

Note 2: Pulse test

Note 3: Surface mounted on 1 1n^2 copper pad of FR4 board; 270℃/W when mounted on min. copper pad

Typical Characteristics

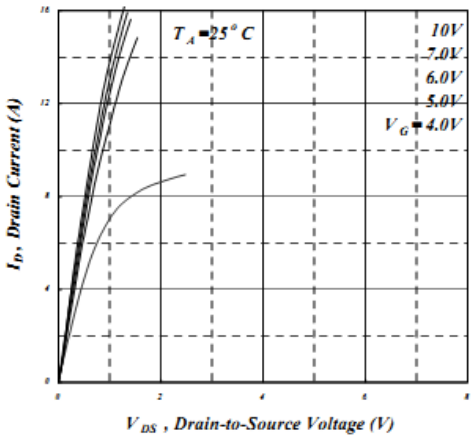


Fig 1. Typical Output Characteristics

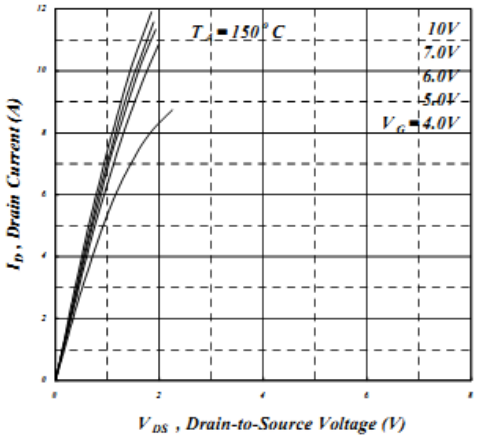


Fig 2. Typical Output Characteristics

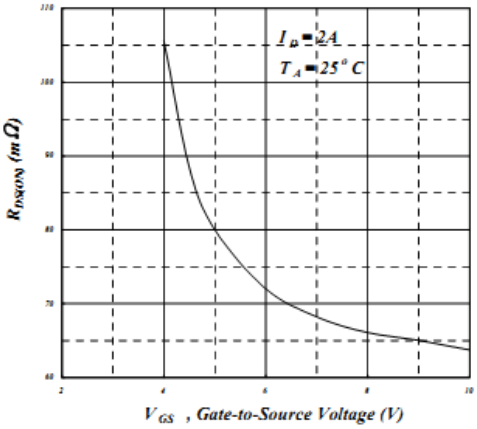


Fig 3. On-Resistance v.s. Gate Voltage

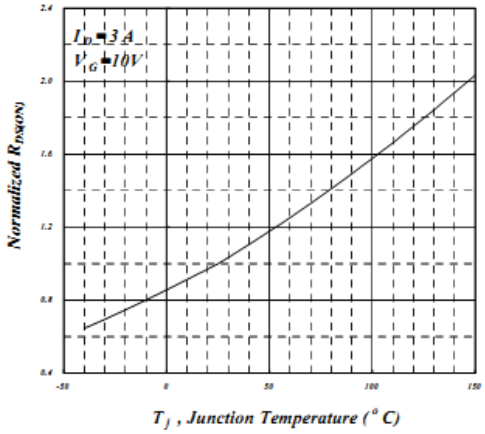


Fig 4. Normalized On-Resistance v.s. Junction Temperature

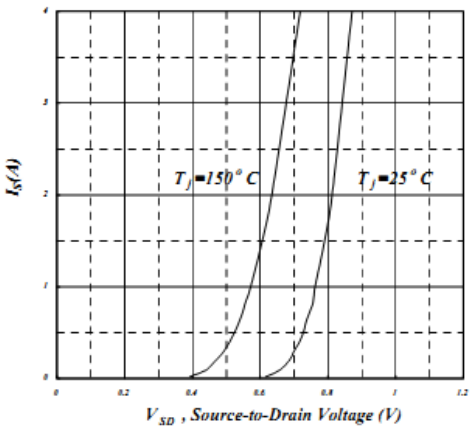


Fig 5. Forward Characteristic of Reverse Diode

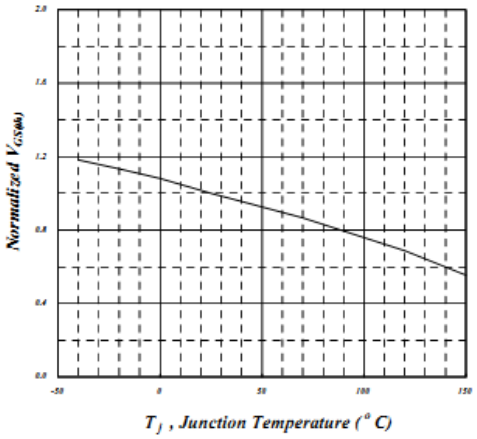


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Typical Characteristics

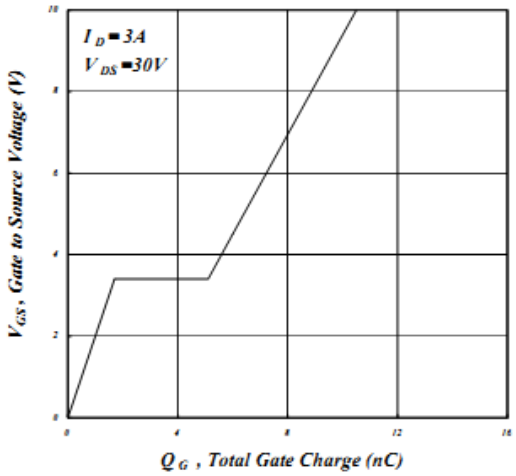


Fig 7. Gate Charge Characteristics

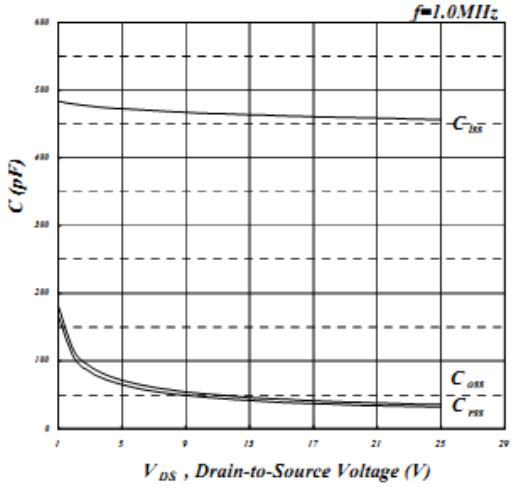


Fig 8. Typical Capacitance Characteristics

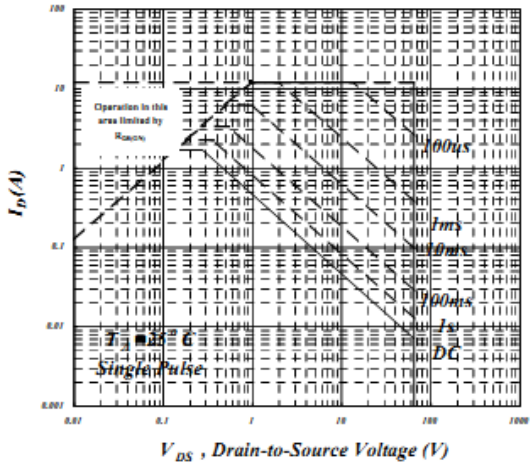


Fig 9. Maximum Safe Operating Area

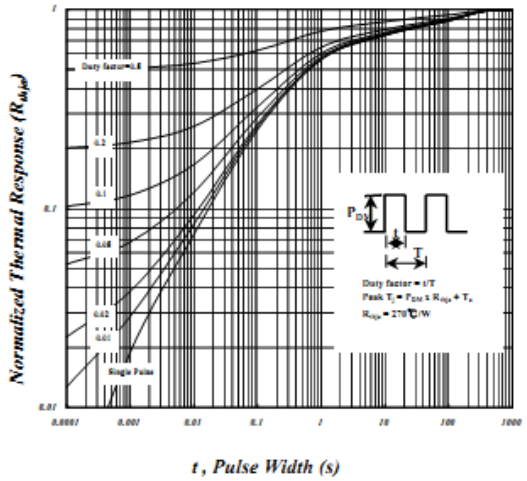


Fig 10. Effective Transient Thermal Impedance

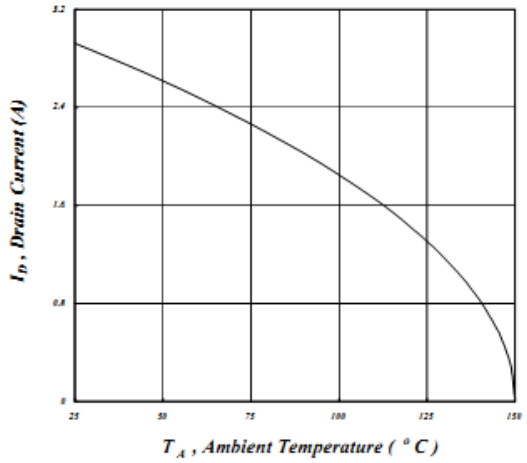


Fig 11. Maximum Continuous Drain Current v.s. Ambient Temperature

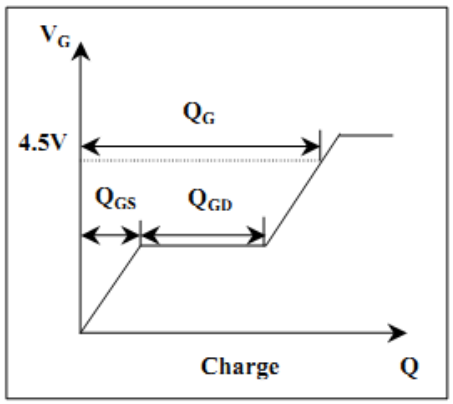
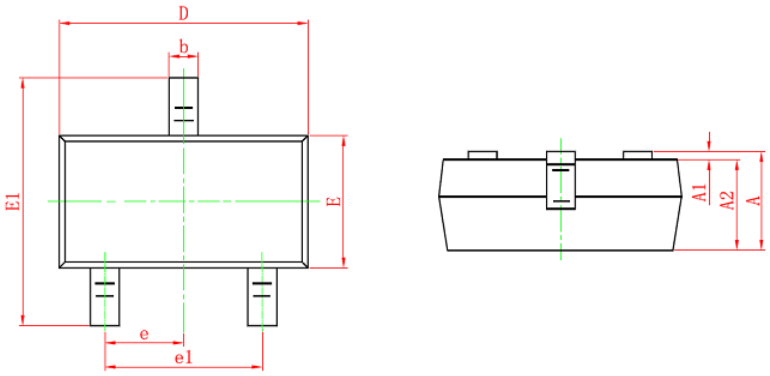
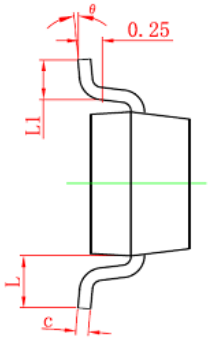


Fig 12. Gate Charge Waveform

Package Outline Dimension

SOT-23





Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

SHANGHAI SINO-IC MICROELECTRONICS CO., LTD

Add: Building 3, Room 3401-03, No.200 Zhangheng Road, ZhangJiang Hi-Tech Park, Pudong, Shanghai 201203, China

Phone: +86-21-33932402 33932403 33932405 33933508 33933608

Fax: +86-21-33932401

Email: webmaster@sino-ic.com

Website: http://www.sino-ic.com