

SE4060B

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- I Simple Drive Requirement
- I Small Package Outline
- I Surface Mount Device

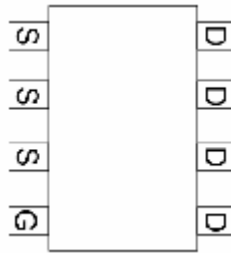
Features

For a single MOSFET

- I $V_{DS} = 40V$
- I $R_{DS(ON)} = 7m\Omega @ V_{GS}=10V$

Pin configurations

See Diagram below



Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	60	A
	Pulsed		200	
Total Power Dissipation	@ TA=25°C	P_D	65	W
Operating Junction Temperature Range		T_J	-55 to 175	°C

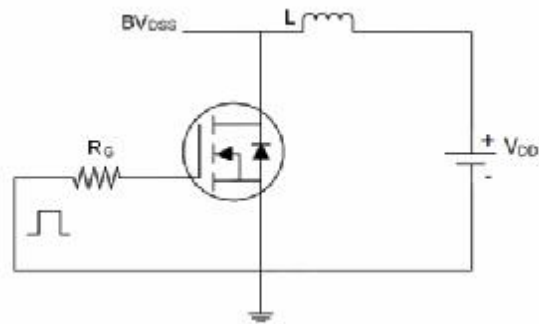
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Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	40	45		V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 40V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20 V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	1.2	1.6	2.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A	-	7	13	mΩ
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =20A	15			S
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		1800		pF
C _{oss}	Output Capacitance			280		pF
C _{rss}	Reverse Transfer Capacitance			190		pF
SWITCHING PARAMETERS						
t _{d(on)}	Turn-On Delay Time	V _{DD} =20V, R _L =1Ω R _G =3Ω		6.4		ns
t _{d(off)}	Turn-Off Delay Time			29.6		ns
t _{d(r)}	Turn-On Rise Time			17.2		ns
t _{d(f)}	Turn-Off Fall Time			16.8		ns
Thermal Resistance						
Symbol	Parameter	Typ	Max	Units		
R _{θJA}	Junction to Ambient (each bin with recommended lands)	-	2.3	°C/W		

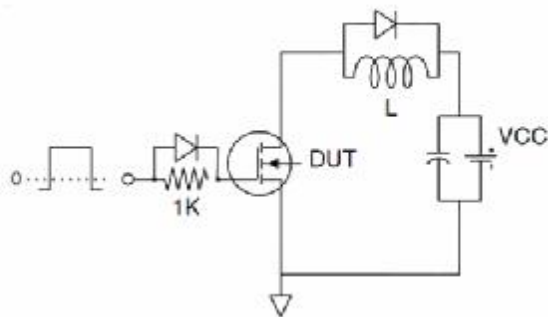
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Test Circuit

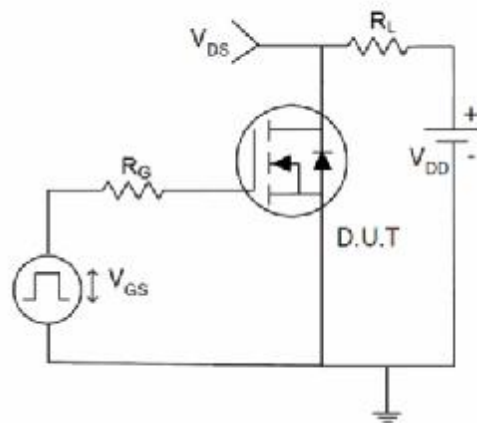
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Characteristics

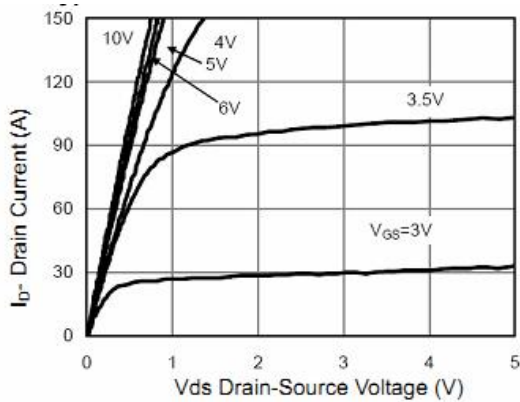


Figure 1 Output Characteristics

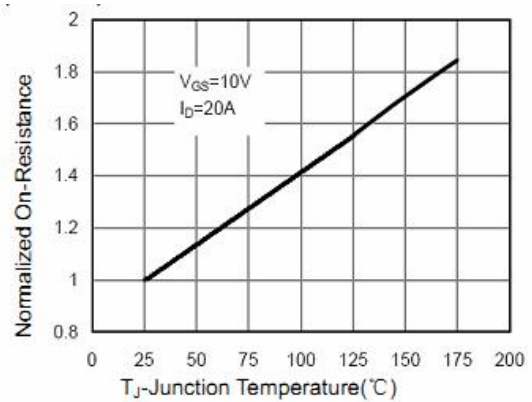


Figure 4 R_{dson} -Junction Temperature

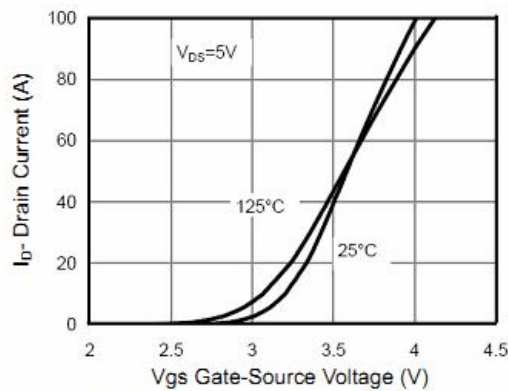


Figure 2 Transfer Characteristics

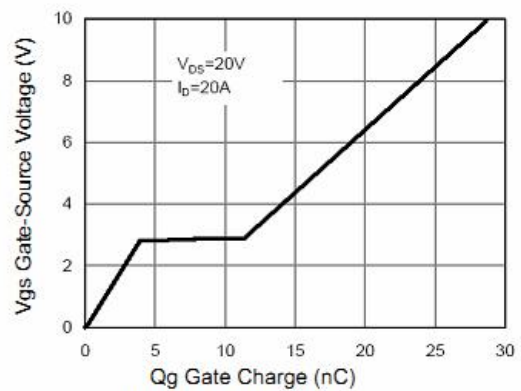


Figure 5 Gate Charge

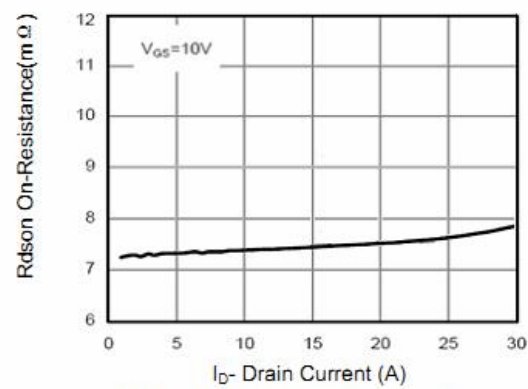


Figure 3 R_{dson} - Drain Current

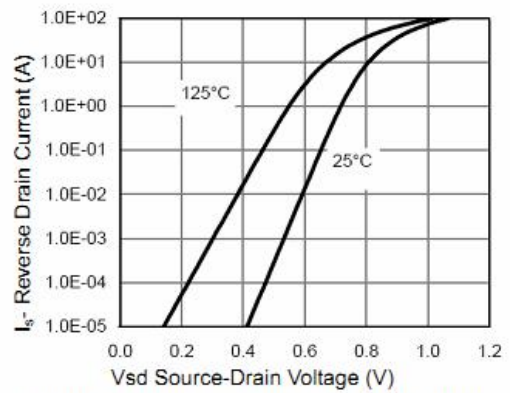


Figure 6 Source- Drain Diode Forward

Typical Characteristics

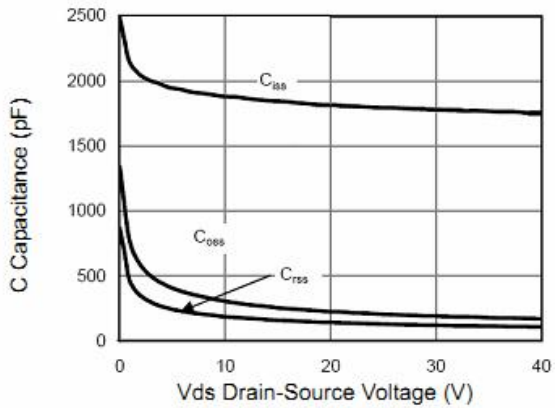


Figure 7 Capacitance vs Vds

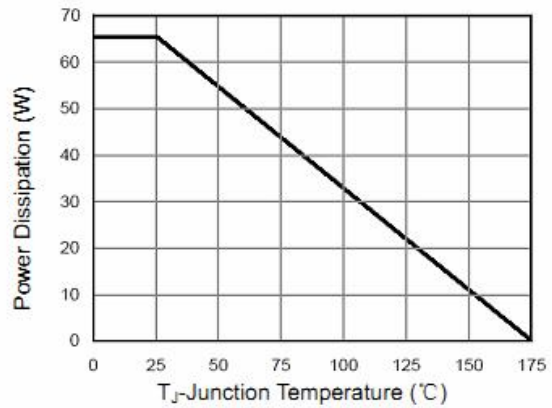


Figure 9 Power De-rating

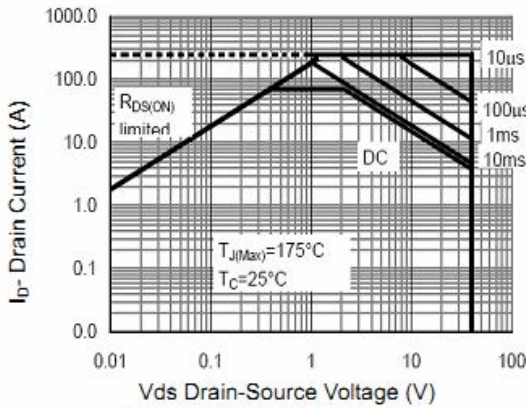


Figure 8 Safe Operation Area

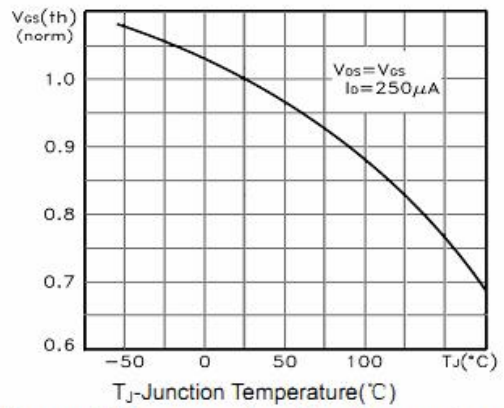


Figure 10 $V_{GS(th)}$ vs Junction Temperature

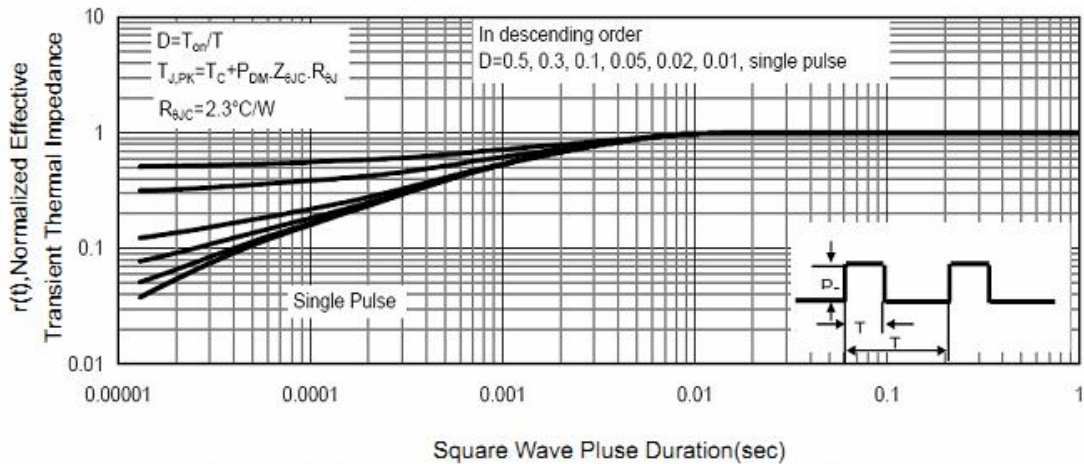
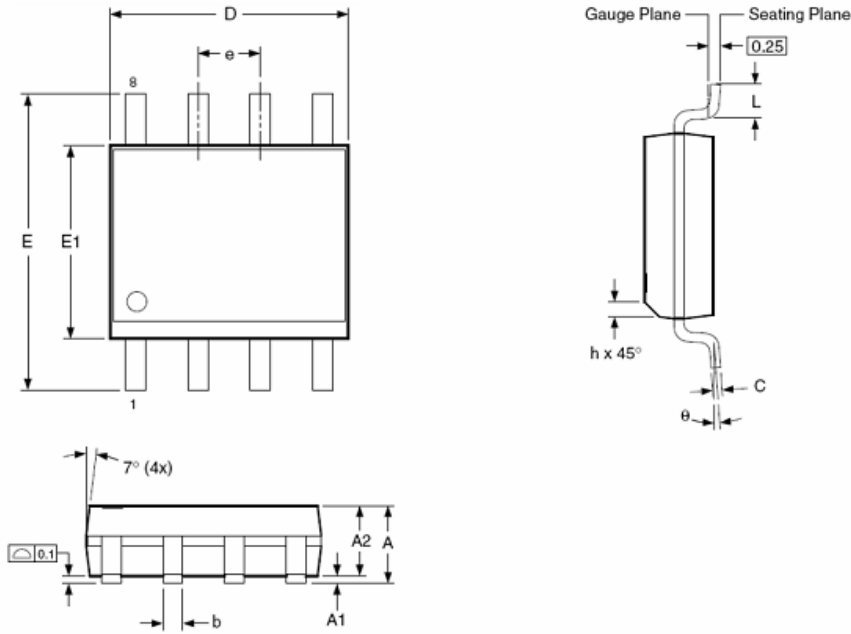


Figure 11 Normalized Maximum Transient Thermal Impedance

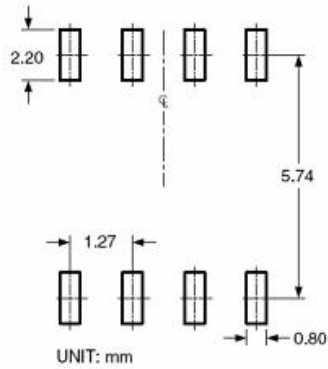
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Package Outline Dimension

SOP-8



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

NOTES:

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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