SHANGHAI SINO-IC
MICROELECTRONICS CO., LTD.

SE10080GK

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

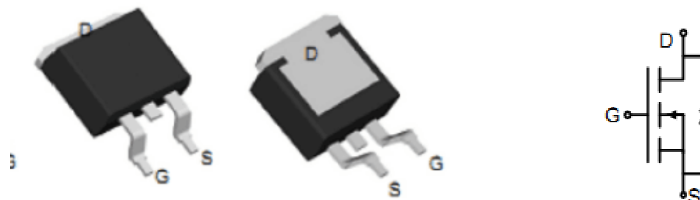
Features

For a single MOSFET

- V_{DS} = 100V
- $R_{DS(ON)}$ = 7.2mΩ @ V_{GS}=10V

Pin configurations

See Diagram below



Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	70	A
	Pulsed		280	
Avalanche Current		I_{AS}	46	A
Avalanche Energy L=0.1mH		E_{AS}	105	mJ
Total Power Dissipation	@TA=25℃	P_D	100	W
Operating Junction Temperature Range		T_J	-55 to 175	℃

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	100	115		V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=100V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	2.2	3.0	3.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=35A	-	7.2	9.0	mΩ
		V_{GS}=6V, I_D=18A	-	8.5	11.0	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=35A		90		S
Rg	Gate Resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz		1.4	2.1	Ω
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, f=1MHz		4550		pF
C_{oss}	Output Capacitance			360		pF
C_{rss}	Reverse Transfer Capacitance			230		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=10V, V_{DS}=50V, I_D=35A		92		nC
Q_{gs}	Gate Source Charge			20		nC
Q_{gd}	Gate Drain Charge			36		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=50V, R_{GEN}=1.6Ω I_D=35A		20		ns
$t_{d(off)}$	Turn-Off Delay Time			50		ns
$t_{d(r)}$	Turn-On Rise Time			45		ns
$t_{d(f)}$	Turn-Off Fall Time			37		ns

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
$R_{θJC}$	Thermal Resistance Junction to Case(t≤10s)	-	1.5	℃/W

Typical Characteristics

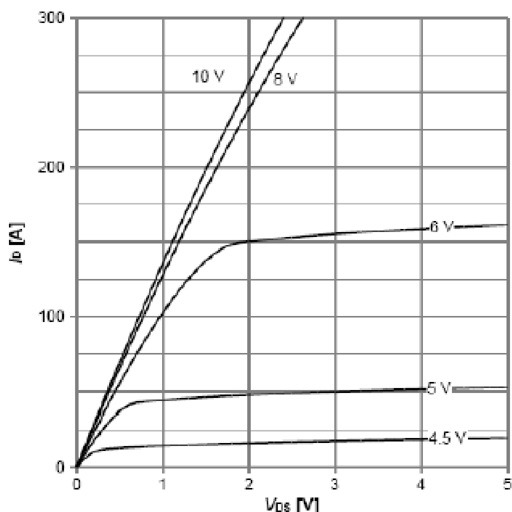


Figure 1: On-Region Characteristics

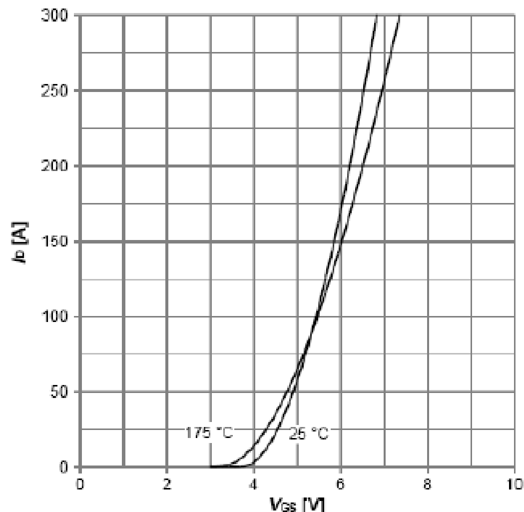


Figure 2: Transfer Characteristics

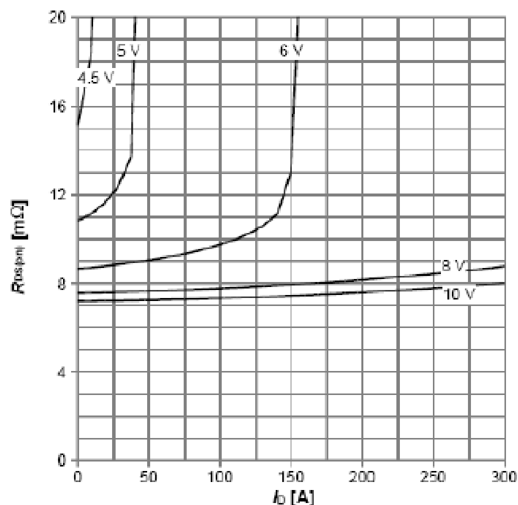


Figure 3: On-Resistance vs Drain current and Gate voltage

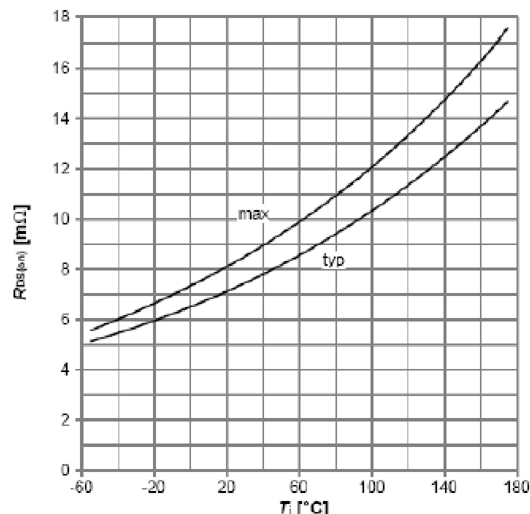


Figure 4: On-Resistance vs Junction Temperature

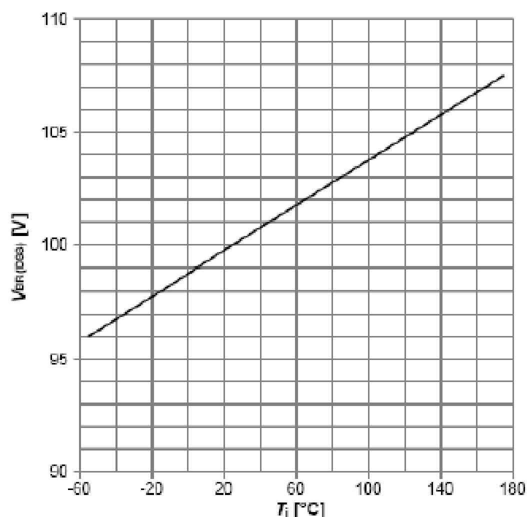


Figure 5: Drain-Source breakdown voltage

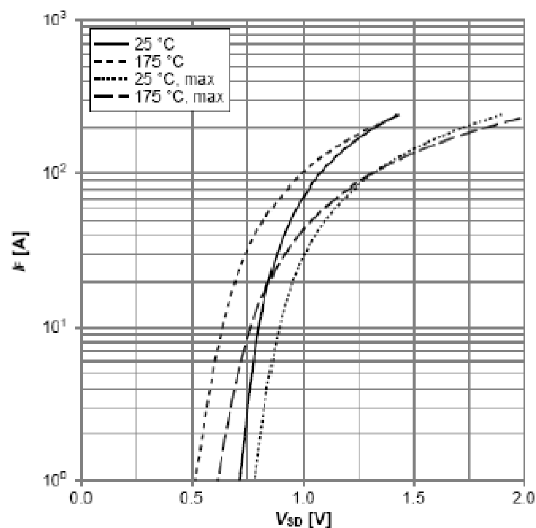


Figure 6: Body-Diode Characteristics

Typical Characteristics

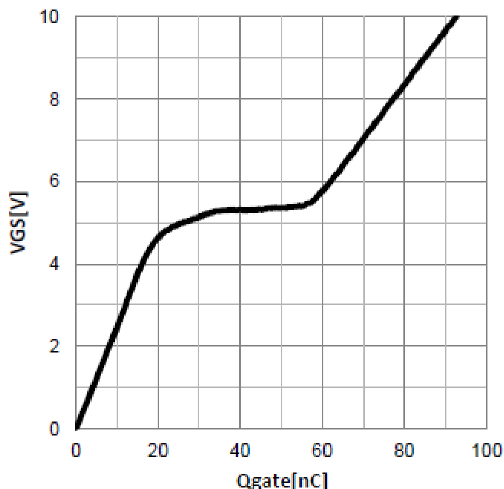


Figure 7: Gate-Charge Characteristics

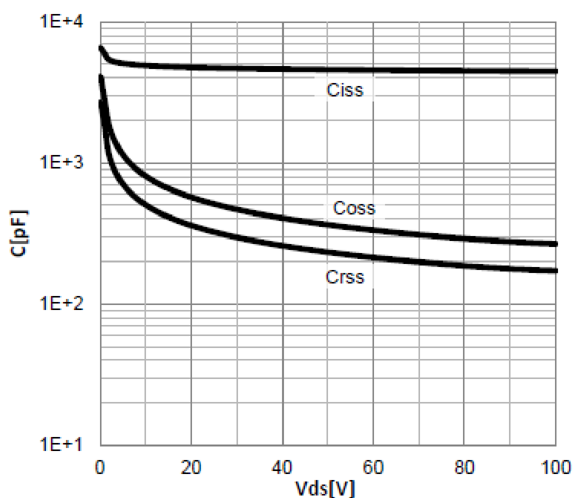


Figure 8: Capacitance Characteristics

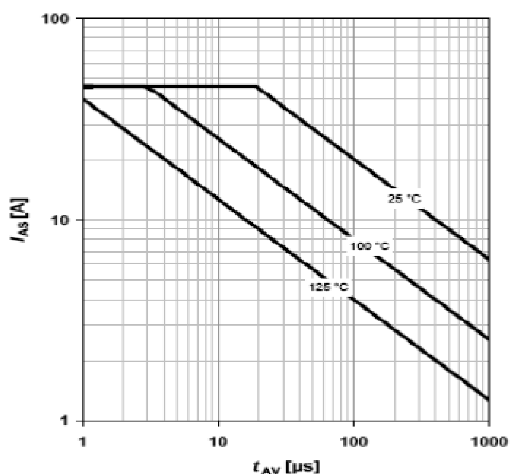


Figure 9: Avalanche Characteristics

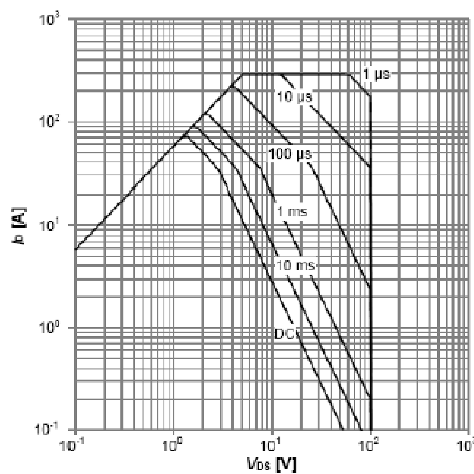


Figure 10: Maximum Forward Biased Safe Operating Area

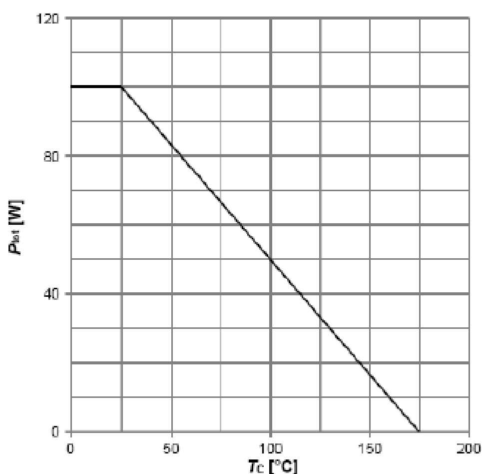


Figure 11: Power dissipation

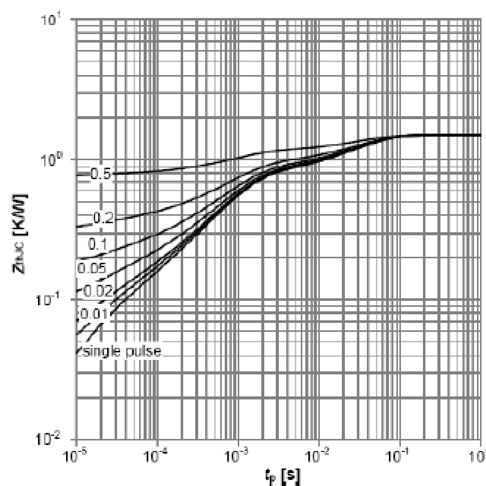


Figure 12: Maximum Transient Thermal Impedance

Package Outline Dimension

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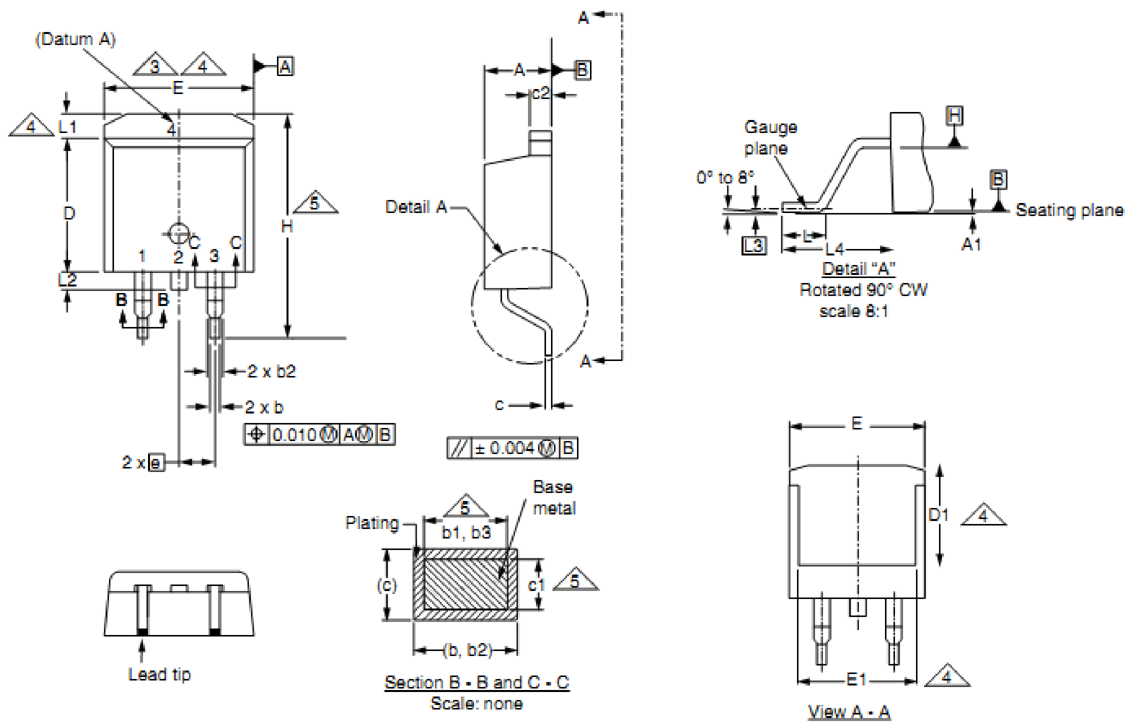

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

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