SHANGHAI SINO-IC
MICROELECTRONICS CO., LTD.

SE80250GD

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

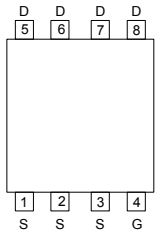
Features

For a single MOSFET

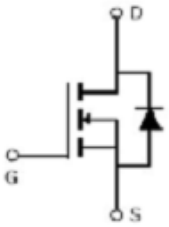
- V_{DS} = 80V
- $R_{DS(ON)}$ = 2.6mΩ @ V_{GS}=10V

Pin configurations

See Diagram below



DFN5*6



Absolute Maximum Ratings

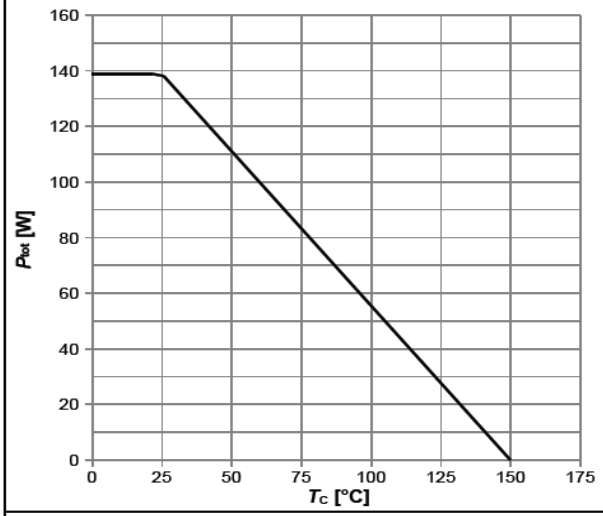
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	100	A
	Pulsed		400	
Single Pulse Avalanche Energy		E_{AS}	250	mJ
Total Power Dissipation	@TC=25℃	P_D	139	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	80			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=100V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	2.2	3.0	3.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=50A	-	2.6	3.0	mΩ
		V_{GS}=6V, I_D=20A		3.4	4.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=50A	55	110		S
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, f=1MHz		4300	5600	pF
C_{oss}	Output Capacitance			700	910	pF
C_{rss}	Reverse Transfer Capacitance			32	56	pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=10V, V_{DS}=40V, I_D=50A		20		nC
Q_{gs}	Gate Source Charge			12		nC
Q_{gd}	Gate Drain Charge			13	19.5	nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=40V, R_{GEN}=3Ω I_D=50A		20		ns
$t_{d(off)}$	Turn-Off Delay Time			43		ns
$t_{d(r)}$	Turn-On Rise Time			12		ns
$t_{d(f)}$	Turn-Off Fall Time			13		ns

Thermal Resistance				
Symbol	**Parameter**	**Typ**	**Max**	**Units**
$R_{\theta JC}$	Thermal Resistance Junction to Case(t≤10s)	-	0.4	℃/W

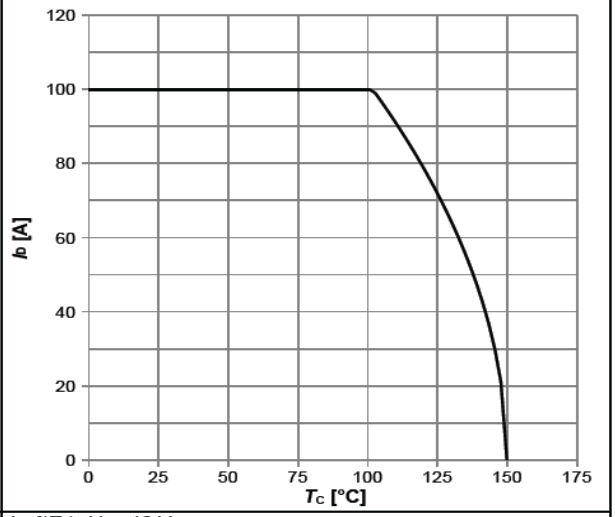
Typical Characteristics

Diagram 1: Power dissipation



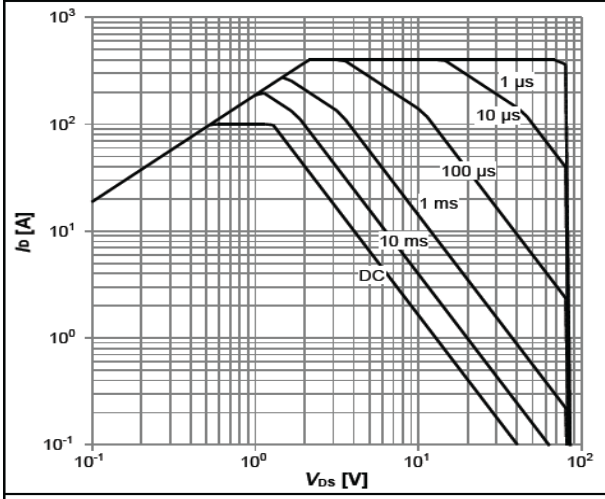
$P_{tot}=f(T_C)$

Diagram 2: Drain current



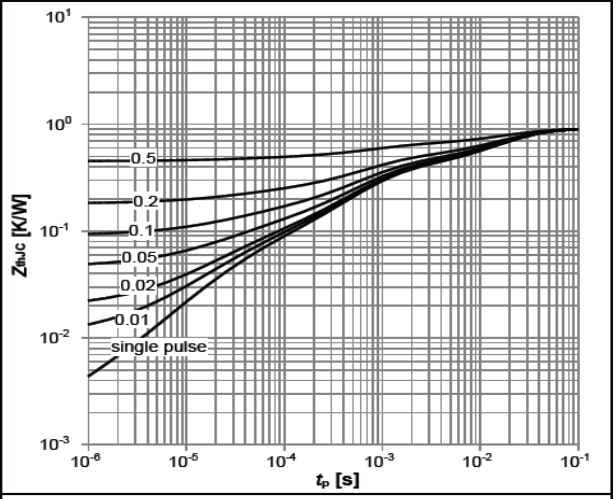
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



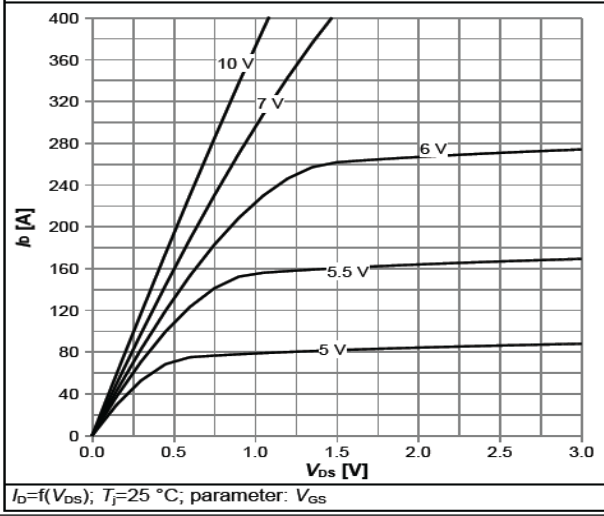
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



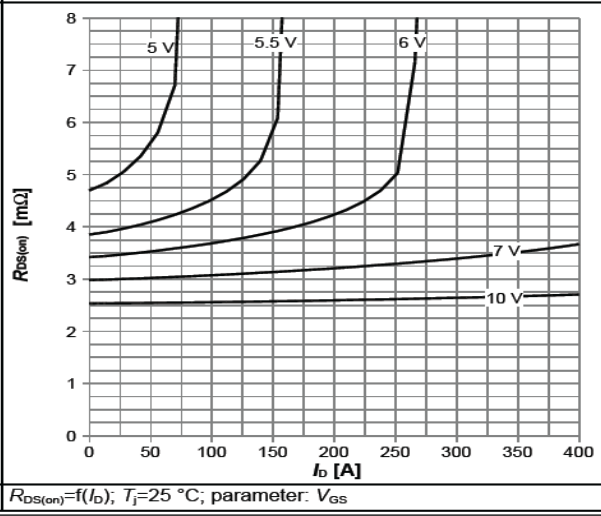
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

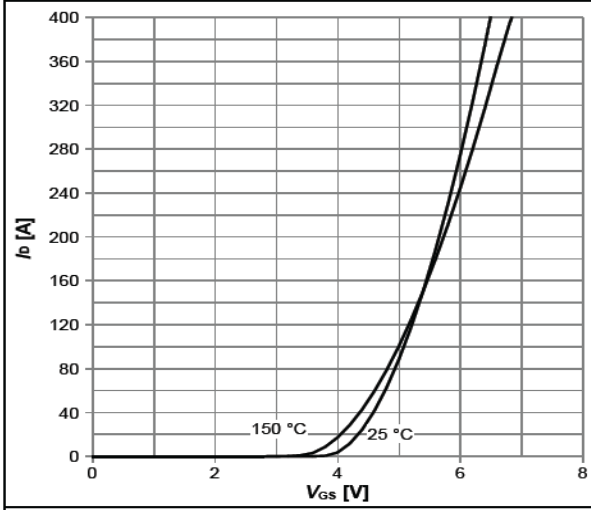
Diagram 6: Typ. drain-source on resistance



$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

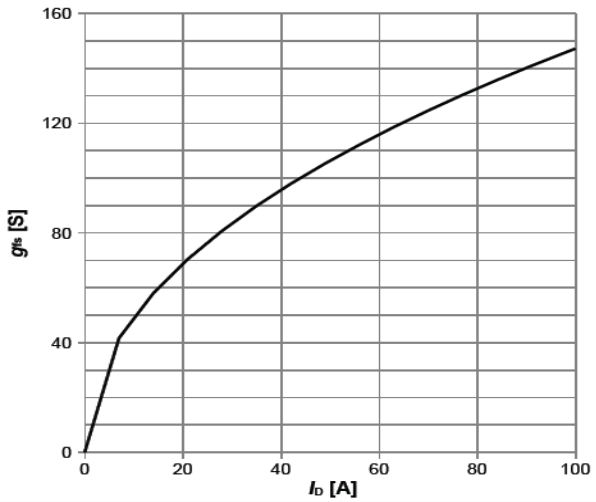
Typical Characteristics

Diagram 7: Typ. transfer characteristics



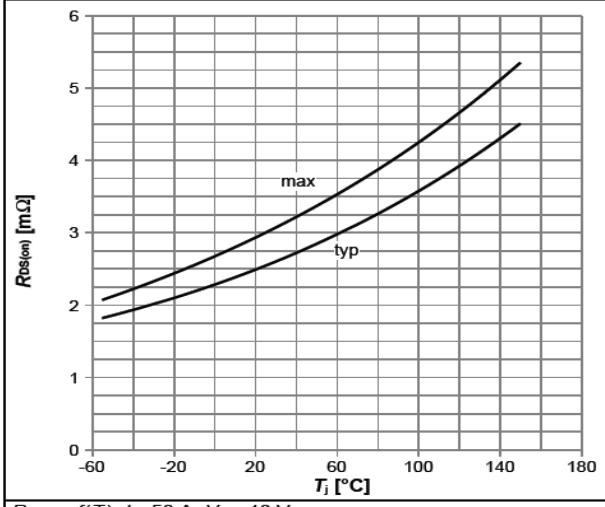
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



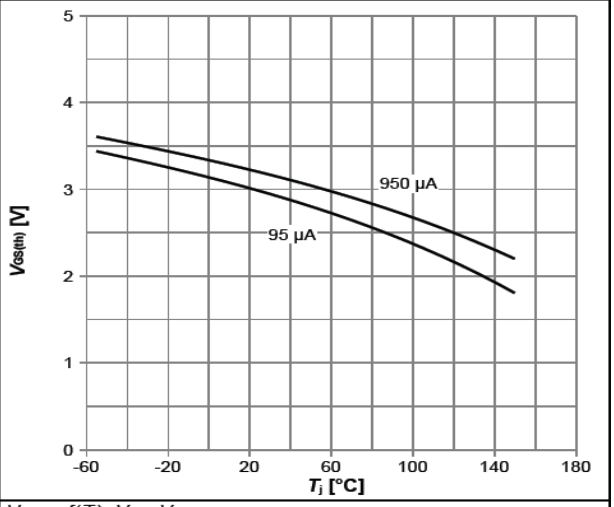
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



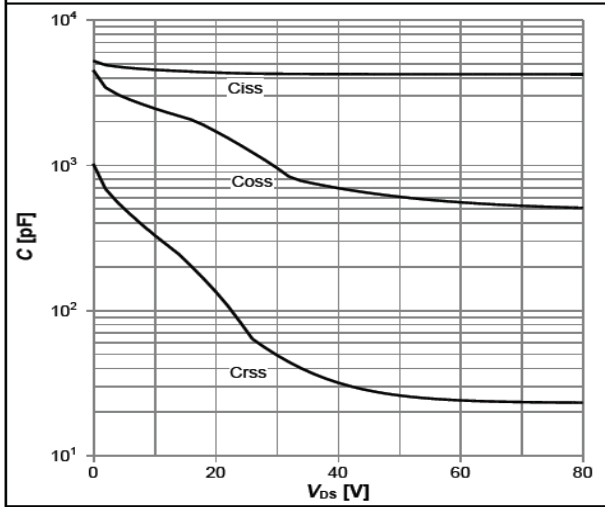
$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



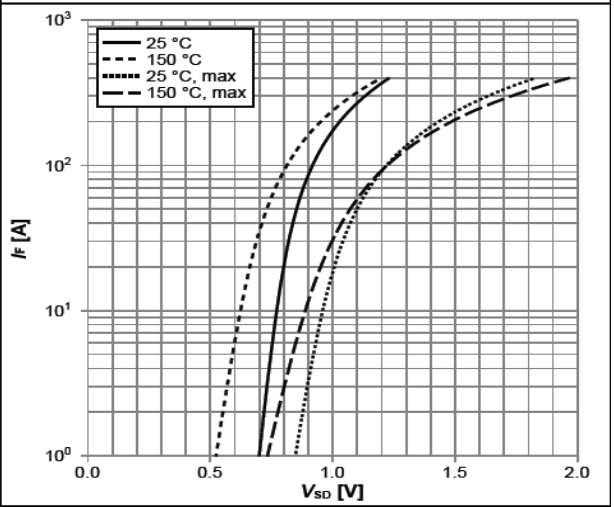
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

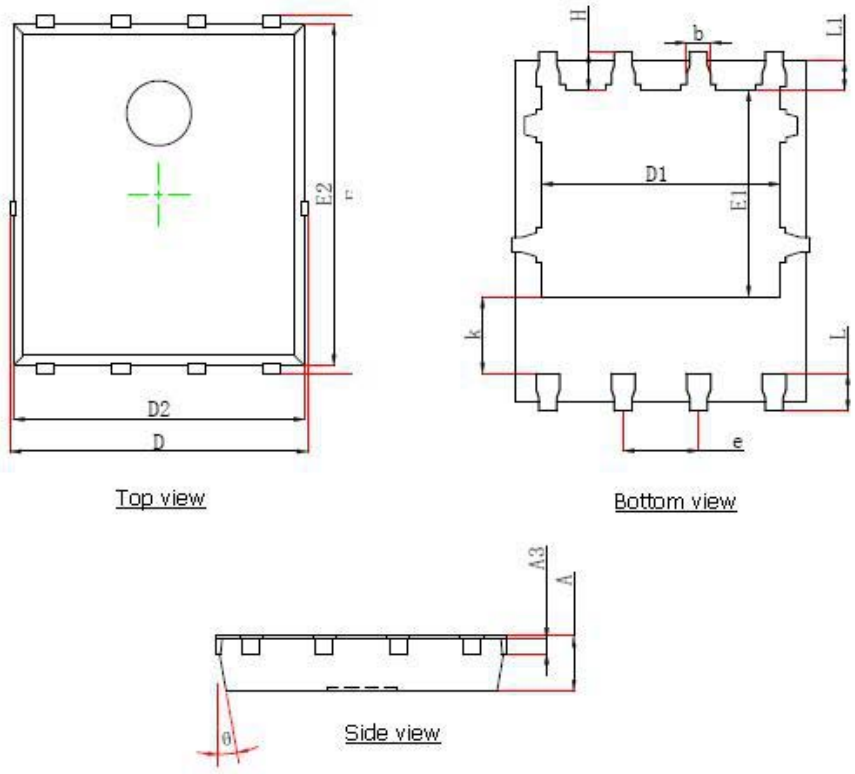
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

Package Outline Dimension

DFN5 × 6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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