SHANGHAI SINO-IC MICROELECTRONICS CO., LTD.

SE0115

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Advanced trench technology to provide excellent RDS(ON), low gate charge and low operation voltage. This device is suitable for using as a load switch or in PWM applications.

- Low $R_{DS(on)}$
- Small Package Outline
- ESD protected

Features

For N-Channel MOSFET

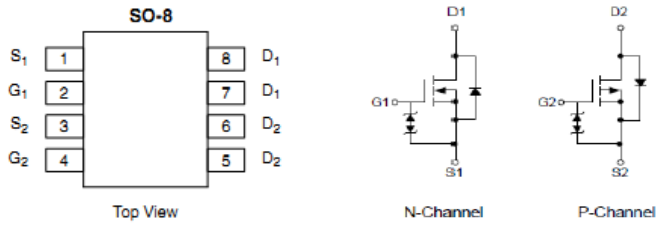
- V_{DS} = 100V
- $R_{DS(ON)}$ = 75mΩ @ V_{GS}=10V

For P-Channel MOSFET

- V_{DS} = -100V
- $R_{DS(ON)}$ =155mΩ @ V_{GS}=-10V

Pin configurations

See Diagram below



Absolute Maximum Ratings

Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	100	-100	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Drain Current	Continuous	I_D	3.5	-2.5	A
	Pulsed		14	-10	
Total Power Dissipation	@TA=25℃	P_D	2	2	W
Operating Junction Temperature Range		T_J	-55 to 175		℃

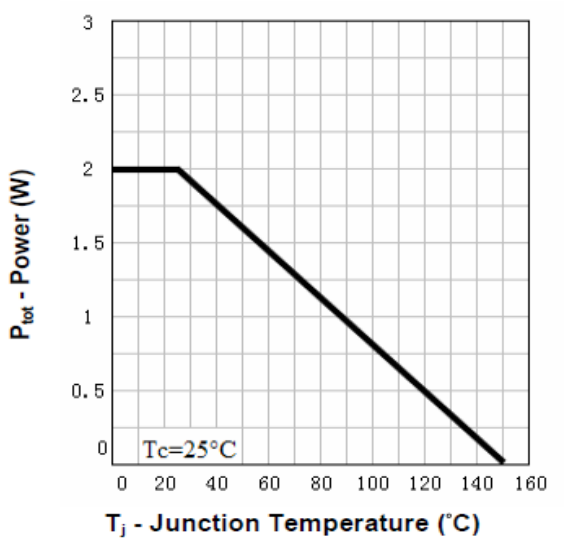
Thermal Resistance

Parameter	Symbol	N-Channel		P-Channel		Units
		Typ	Max	Typ	Max	
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	55	62.5	53	62.5	℃/W

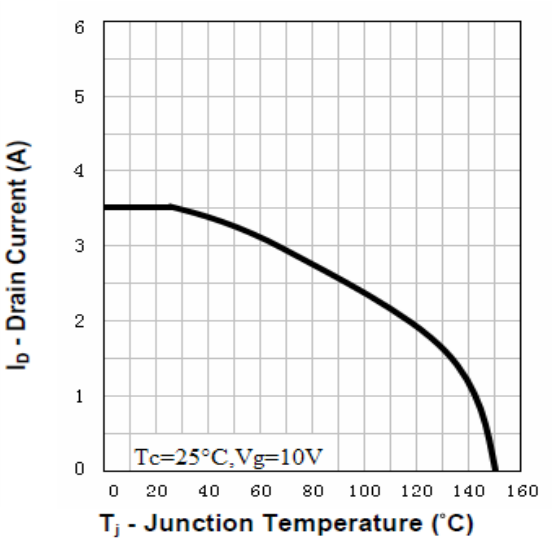
Electrical Characteristics (TJ=25℃ unless otherwise noted)							
Symbol	**Parameter**	**Test Conditions**	**Type**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	N-Ch	100			V
		I_D=250μA, V_{GS}=0 V	P-Ch	-100			
I_{DSS}	Drain to Source Leakage Current	V_{DS}= 100V, V_{GS}=0V	N-Ch			1	μA
		V_{DS}= -100V, V_{GS}=0V	P-Ch			-1	
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20V, V_{DS}=0V	N-Ch			10	μA
			P-Ch			-10	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	N-Ch	1.5	2	2.7	V
		V_{DS}= V_{GS}, I_D=-250μA	P-Ch	-1.5	-2	-2.7	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=2A	N-Ch		75	85	mΩ
		V_{GS}=-10V, I_D=-2A	P-Ch		155	170	
		V_{GS}=4.5V, I_D=1.5A	N-Ch		80	95	
		V_{GS}=-4.5V, I_D=-1.5A	P-Ch		175	195	
SWITCHING PARAMETERS							
C_{iss}	Input Capacitance	N-Channel: V_{DS}=50V,V_{GS}=0V,f=1 MHz P-Channel: V_{DS}=-50V,V_{GS}=0V,f=1 MHz	N-Ch		1520		pF
			P-Ch		1630		
C_{oss}	Output Capacitance		N-Ch		134		
			P-Ch		191		
C_{rss}	Reverse Transfer Capacitance		N-Ch		62		
			P-Ch		83		
Q_g	Total Gate Charge	N-Channel: V_{DS}=80V,V_{GS}=10V, I_D=3.5A P-Channel: V_{DS}=-80V,V_{GS}=-10V, I_D=-2.5A	N-Ch		18		nC
			P-Ch		23		
Q_{gs}	Gate Source Charge		N-Ch		4		
			P-Ch		7		
Q_{gd}	Gate Drain Charge		N-Ch		5		
			P-Ch		6		
$t_{d(on)}$	Turn-On Delay Time	N-Channel: V_{DD}=50V,I_D=3.5A, R_{GEN}=6Ω, R_L=30Ω P-Channel: V_{DD}=-50V,I_D=-2.5A, R_{GEN}=10Ω, R_L=30Ω	N-Ch		12		ns
			P-Ch		16		
$t_{d(off)}$	Turn-Off Delay Time		N-Ch		34		
			P-Ch		45		
$t_{d(r)}$	Turn-On Rise Time		N-Ch		24		
			P-Ch		28		
$t_{d(f)}$	Turn-Off Fall Time		N-Ch		18		
			P-Ch		24		

Typical Characteristics(N-Channel)

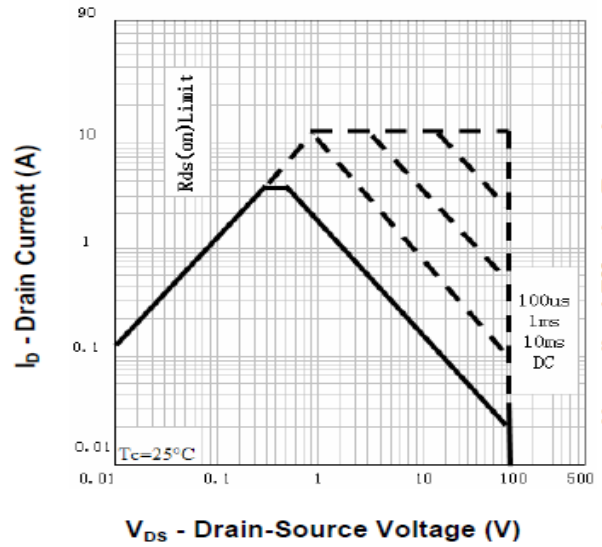
Power Dissipation



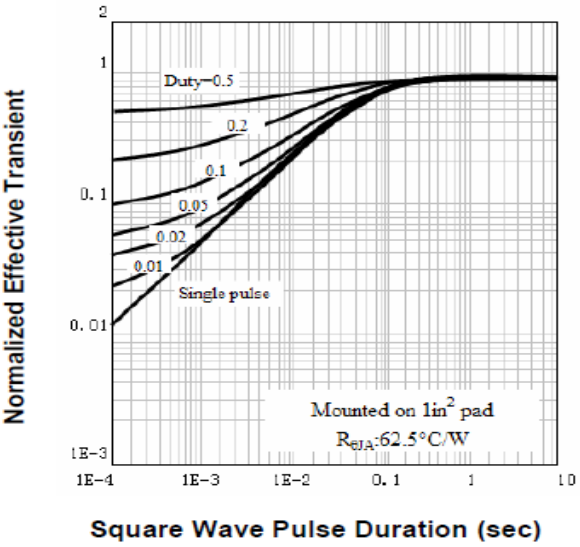
Drain Current



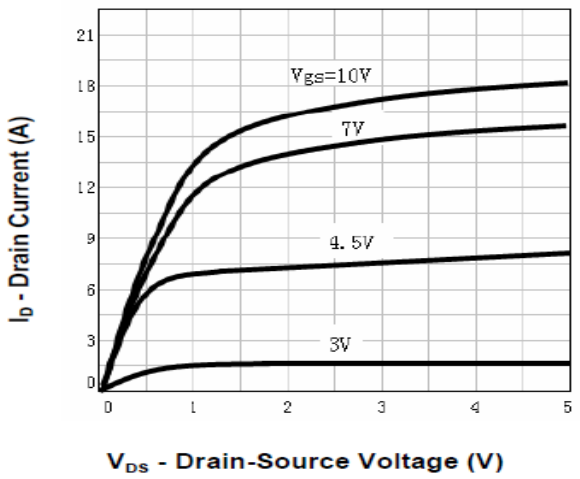
Safe Operation Area



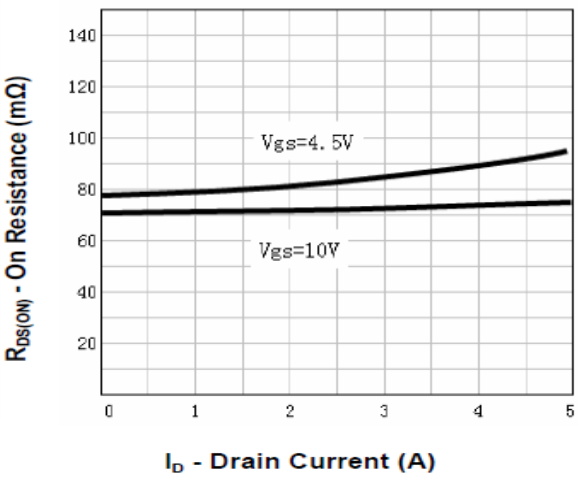
Thermal Transient Impedance



Output Characteristics



Drain-Source On Resistance



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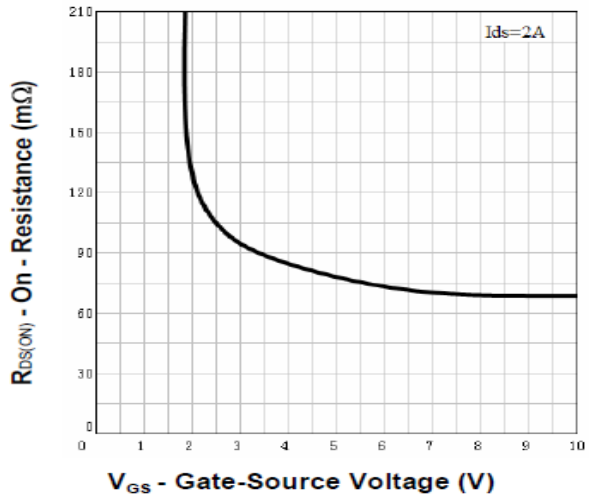
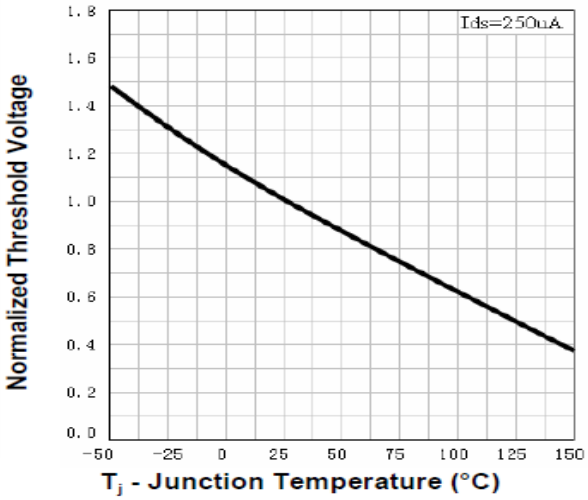
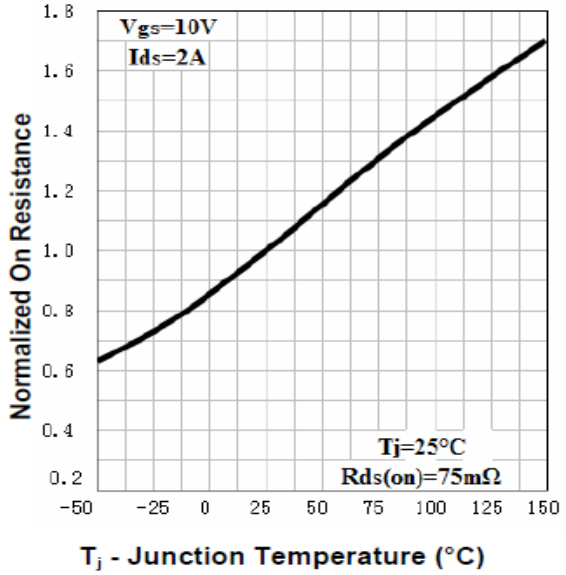
Drain-Source On Resistance



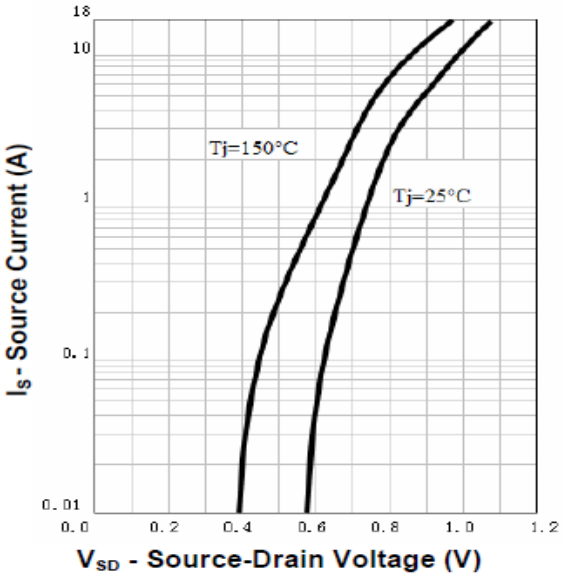
Gate Threshold Voltage



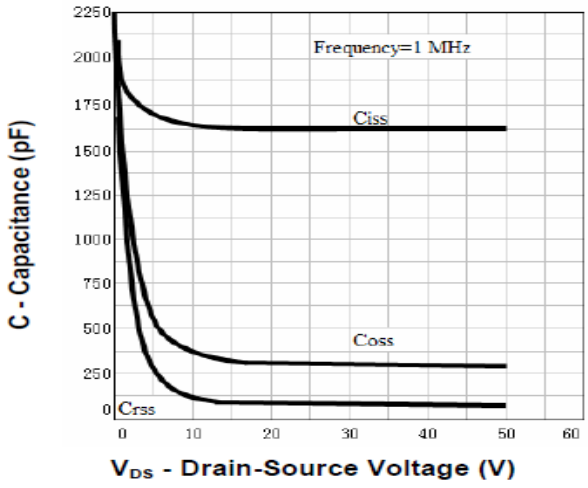
Drain-Source On Resistance



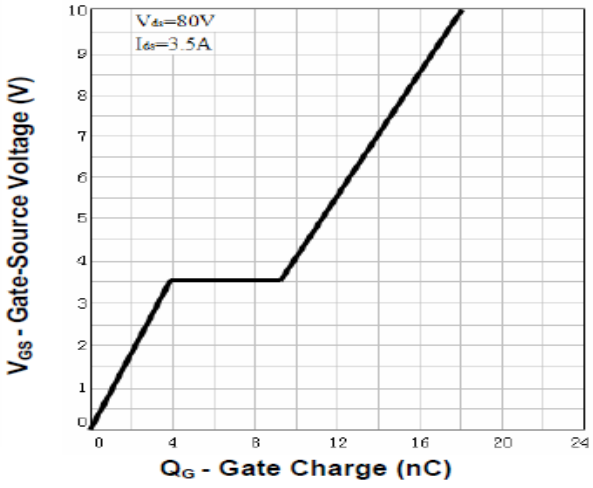
Source-Drain Diode Forward



Capacitance

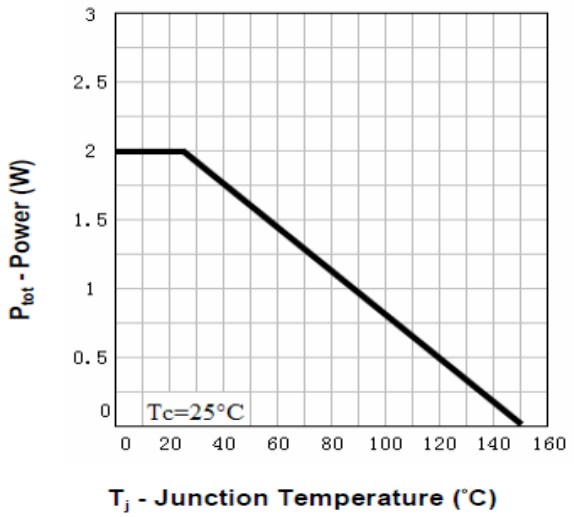


Gate Charge

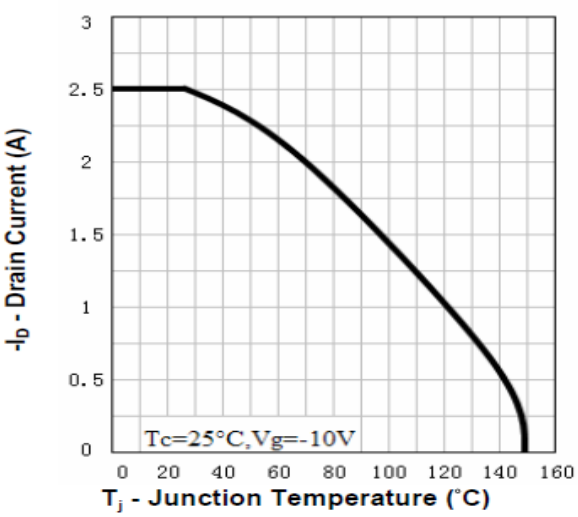


Typical Characteristics(P-Channel)

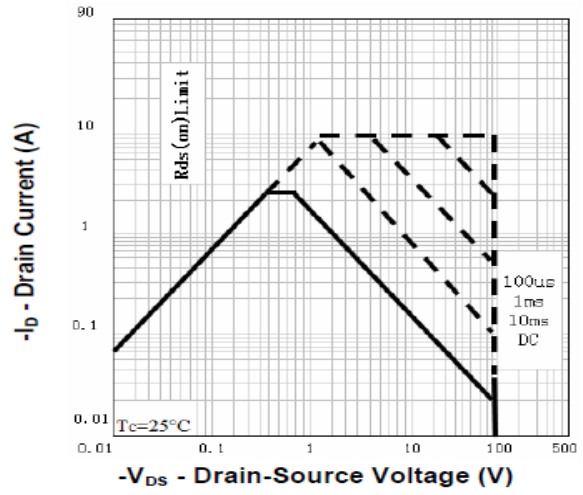
Power Dissipation



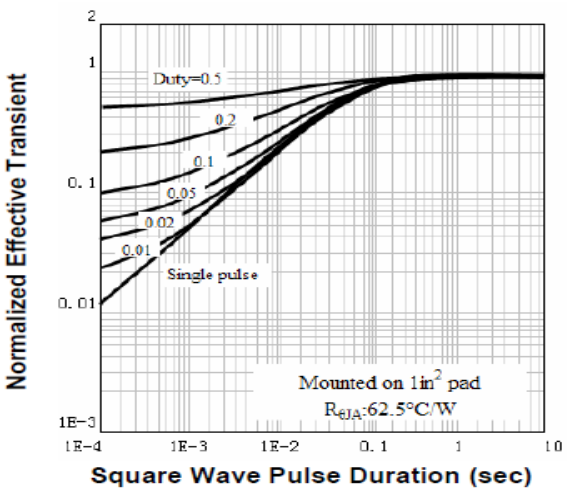
Drain Current



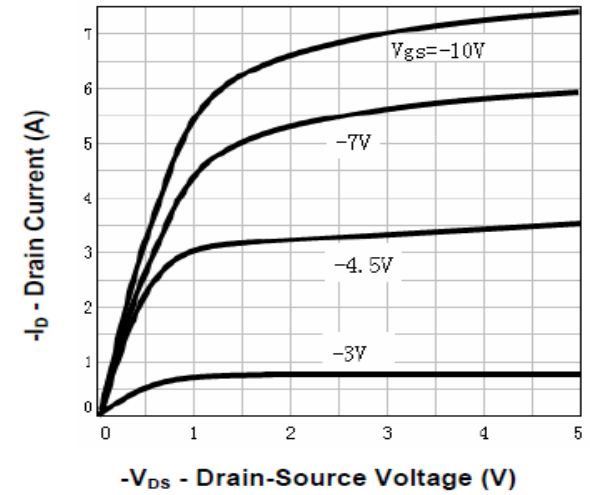
Safe Operation Area



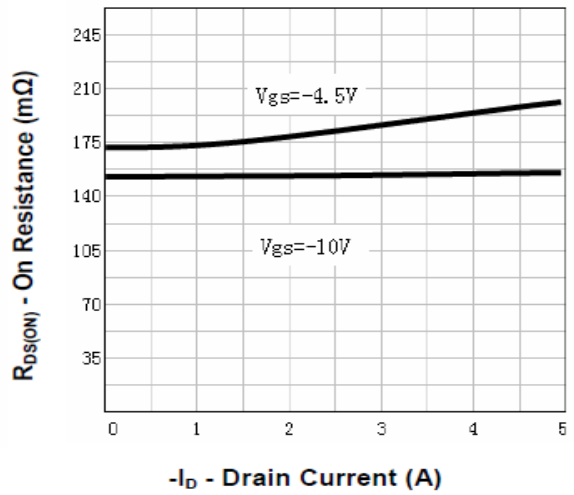
Thermal Transient Impedance



Output Characteristics



Drain-Source On Resistance



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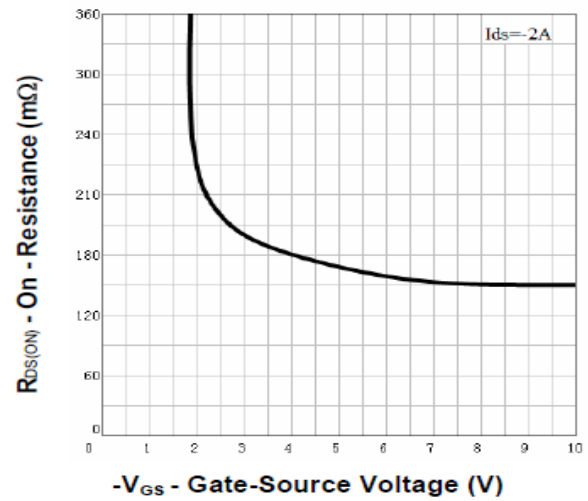
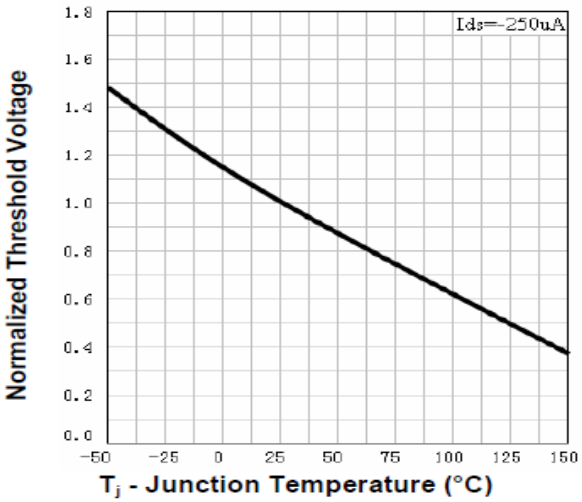


Gate Threshold Voltage



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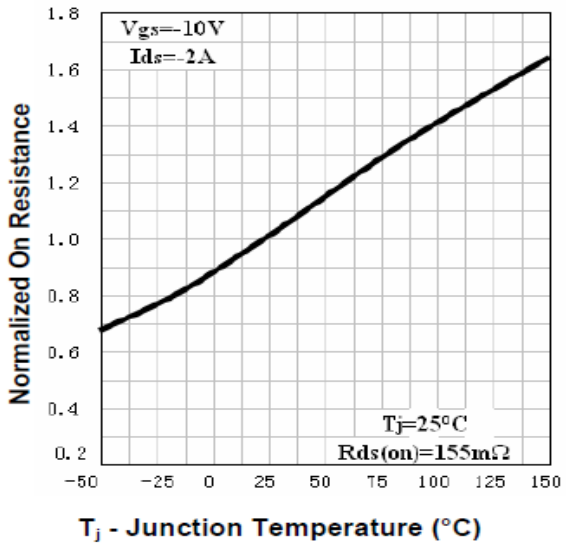
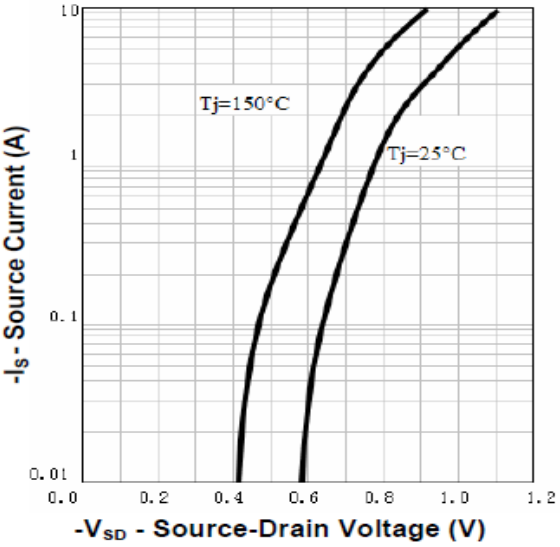
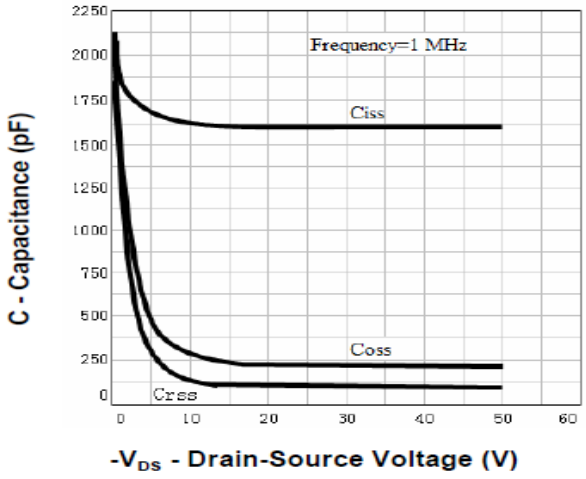


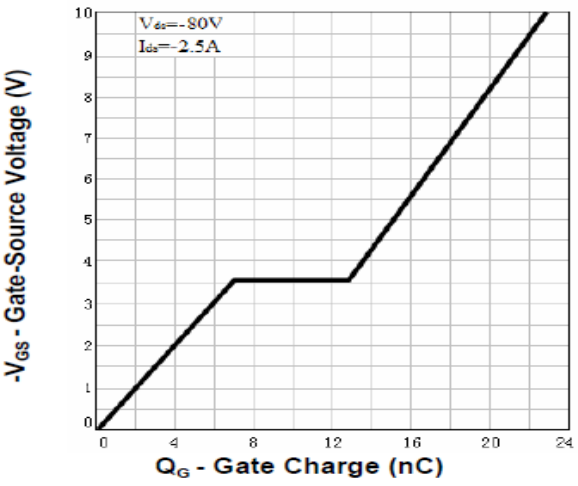
Source-Drain Diode Forward



Capacitance

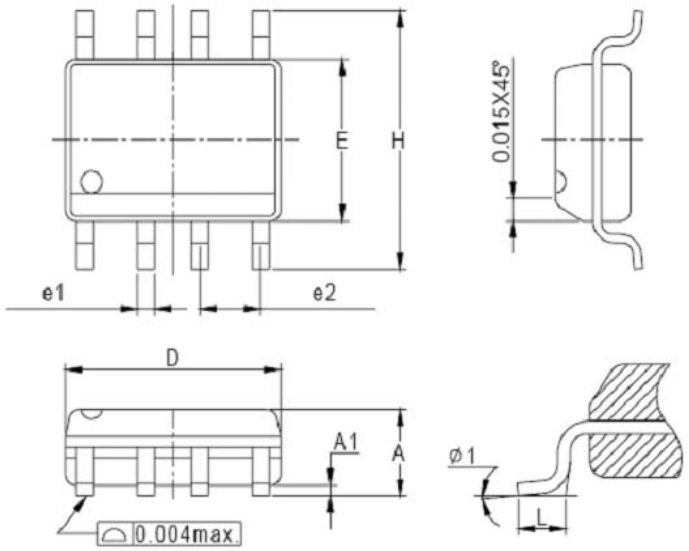


Gate Charge



Package Outline Dimension

SOP-8



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

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