

SE18NS60

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

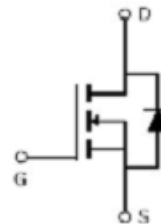
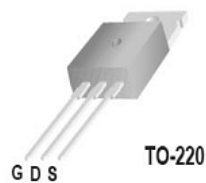
Features

For a single MOSFET

- $V_{DS} = 600V$
- $R_{DS(ON)} = 160m\Omega @ V_{GS}=10V @ I_{DS}=5A$

Pin configurations

See Diagram below



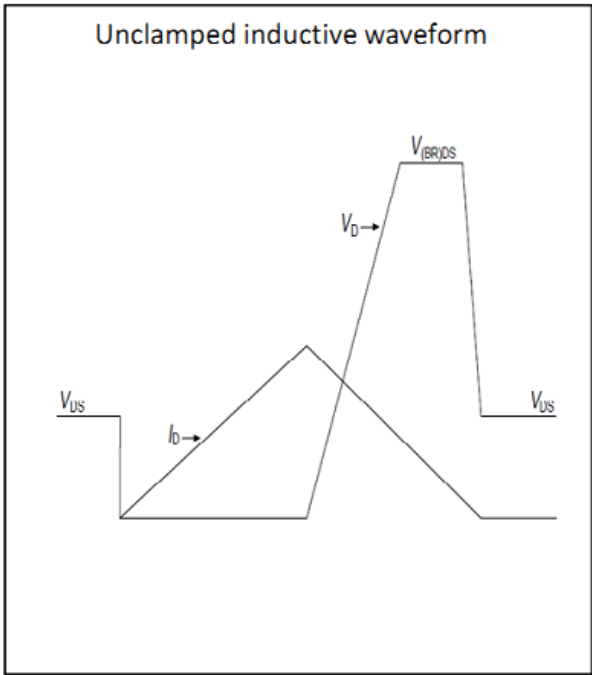
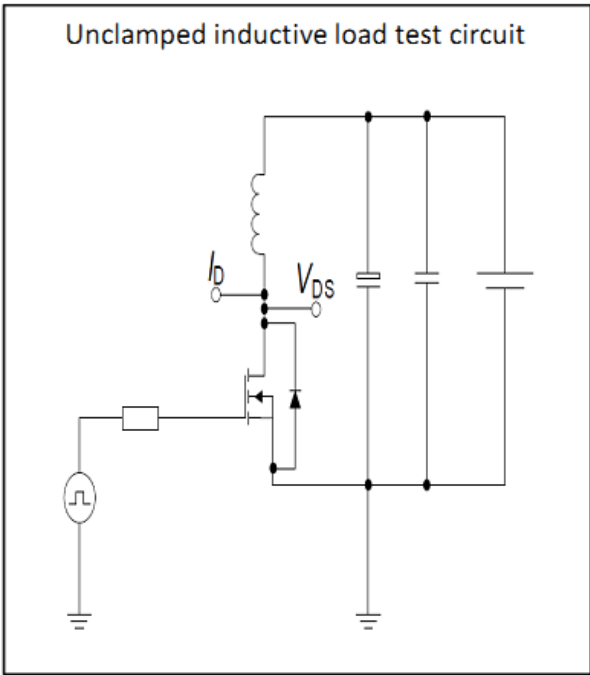
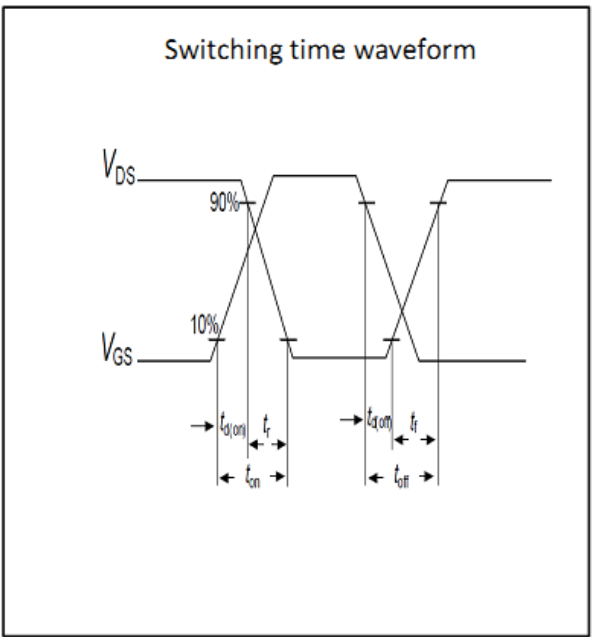
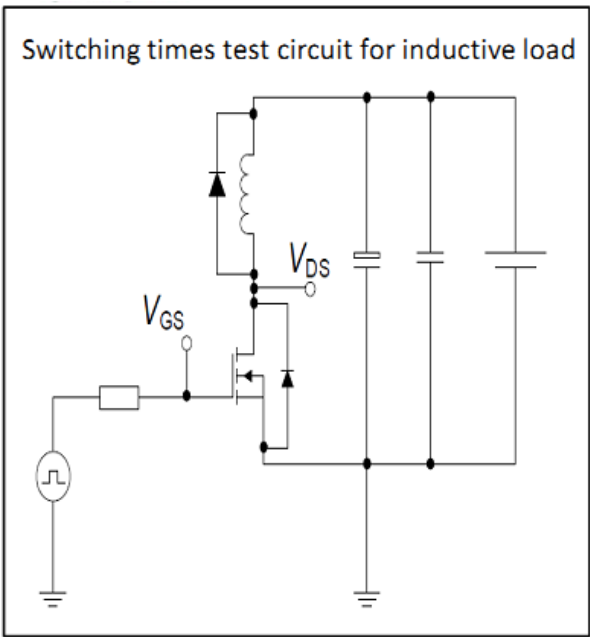
Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	Continuous	I_D	18	A
	Pulsed		55	
Total Power Dissipation	@TA=25°C	P_D	208	W
Operating Junction Temperature Range		T_J	-55 to 150	°C

SE18NS60

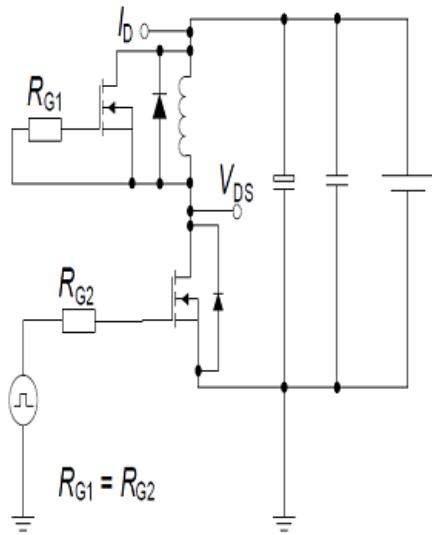
Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	600			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 600V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =30 V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	2.5		4.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A		160	190	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz		1440		pF
C _{oss}	Output Capacitance			300		pF
C _{rss}	Reverse Transfer Capacitance			10		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =480V, I _D =10A		70	90	nC
Q _{gs}	Gate Source Charge			7.8		nC
Q _{gd}	Gate Drain Charge			9		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =400V, R _{GEN} =20Ω I _D =5A		25		ns
t _{d(off)}	Turn-Off Delay Time			70		ns
t _{d(r)}	Turn-On Rise Time			55		ns
t _{d(f)}	Turn-Off Fall Time			40		ns
Thermal Resistance						
Symbol	Parameter	Min	Typ	Units		
R _{θJC}	Junction to Case		0.6	°C/W		
R _{θJA}	Junction to Ambient (t ≤ 10s)		62	°C/W		

Test Circuits and Waveform

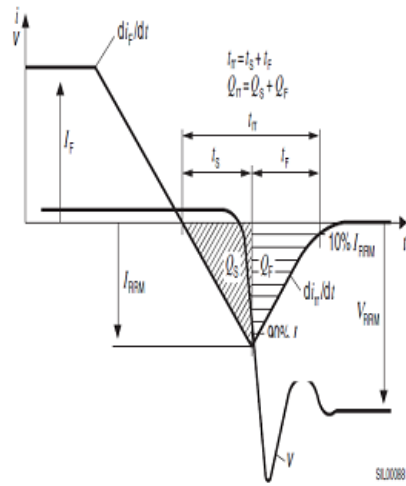


Test Circuits and Waveform

Test circuit for diode characteristics

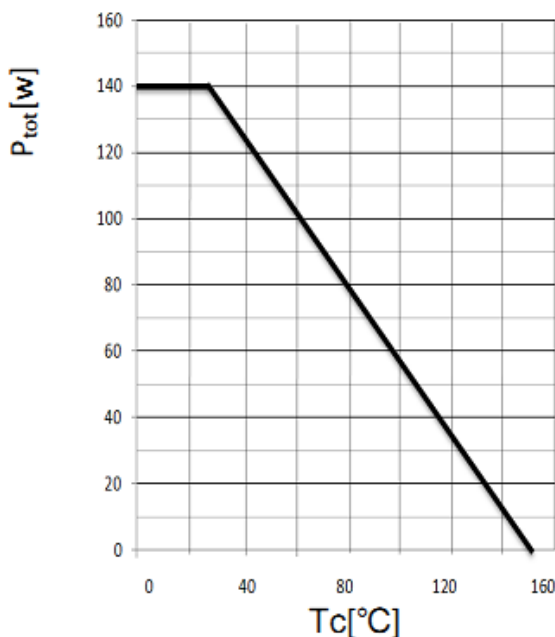


Diode recovery waveform

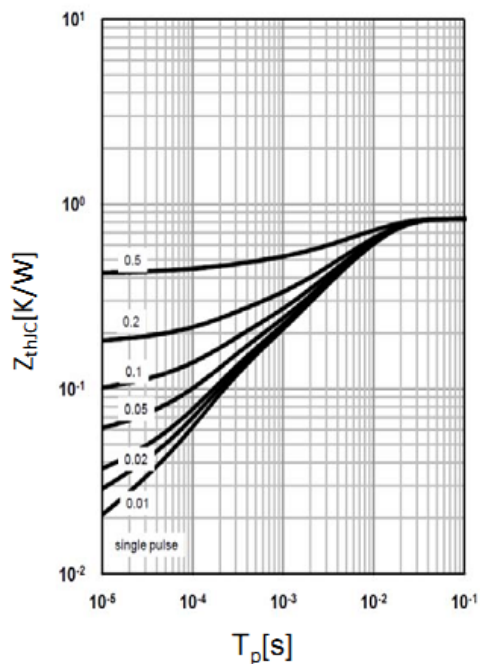


Typical Characteristics

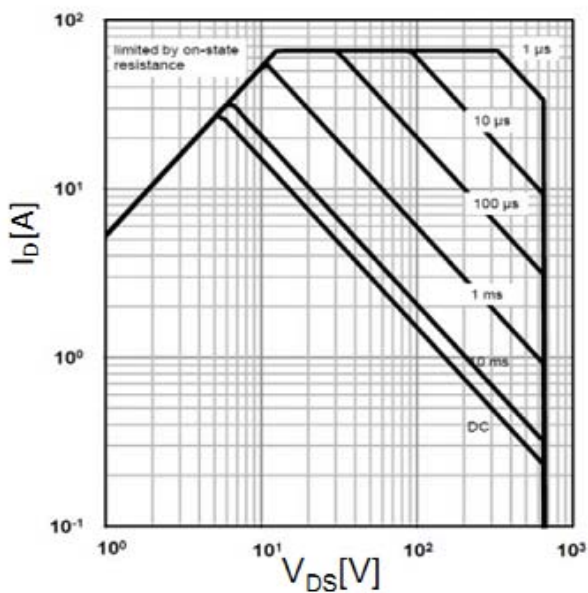
Power dissipation
TO-220P



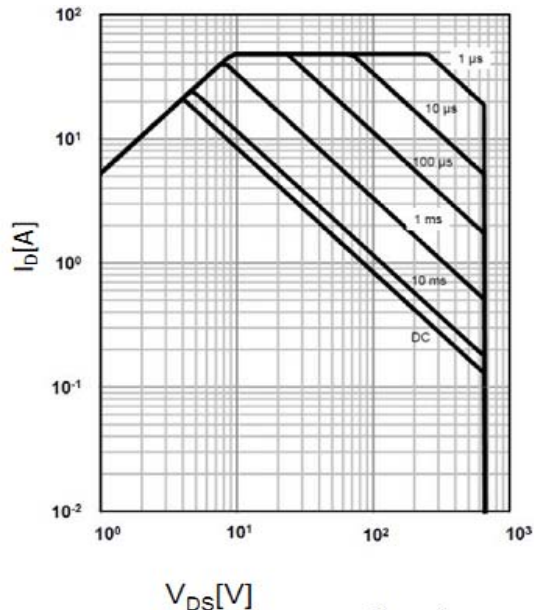
Max. transient thermal impedance
TO-220P



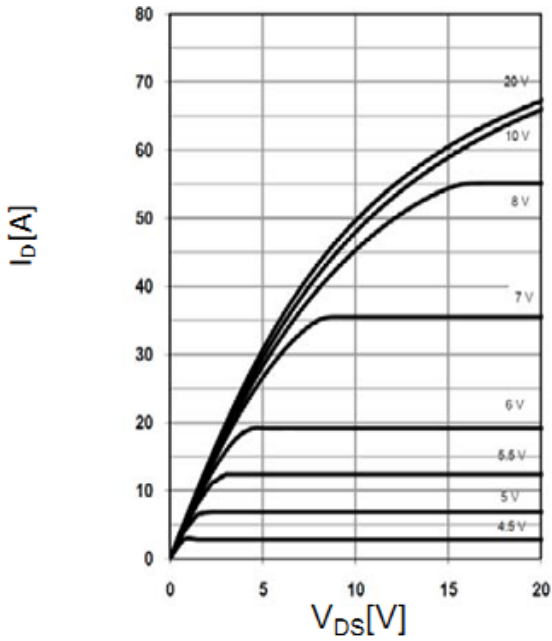
Safe operation area TC=25°C



Safe operation area TC=80°C



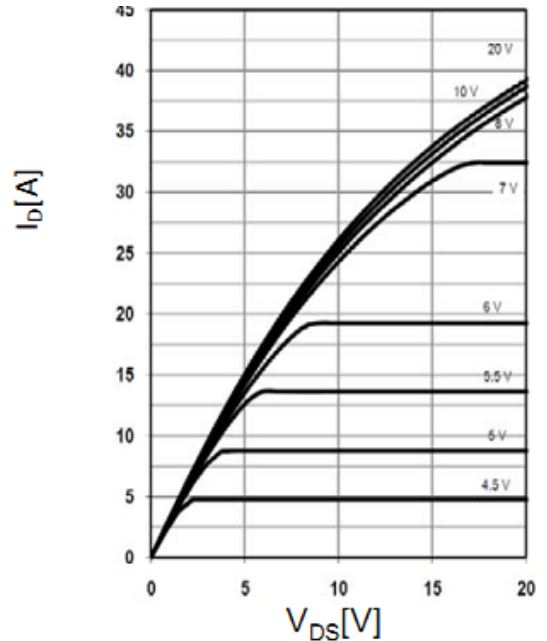
Output characteristics at TC=25°C



$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}; \text{ parameter: } V_{GS}$

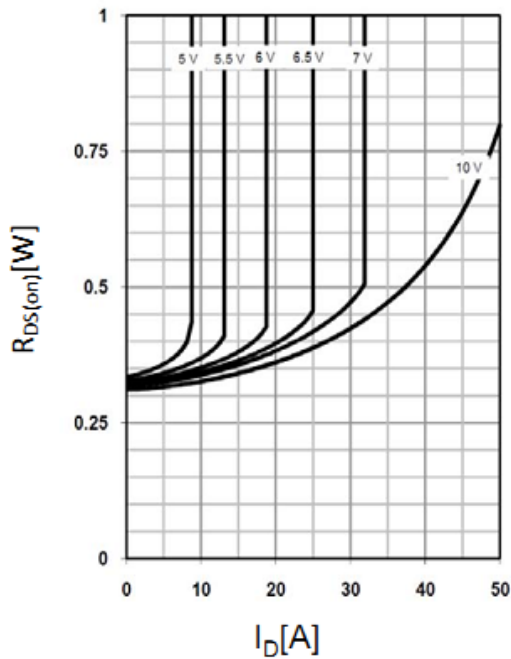
Typ. drain-source on-state resistance

Output characteristics at TC=125°C

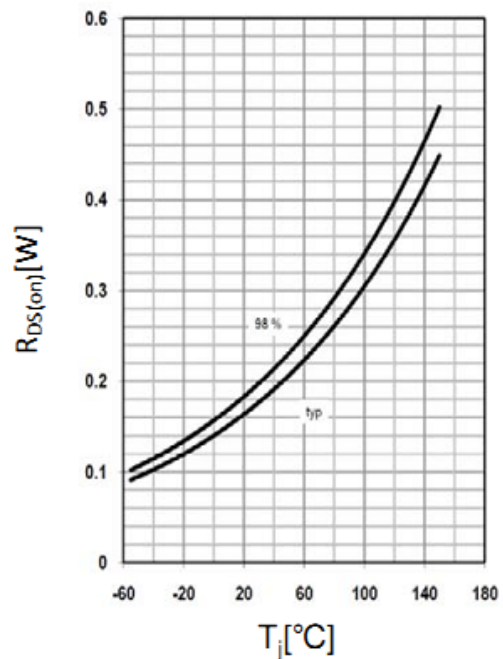


$I_D=f(V_{DS}); T_j=125\text{ }^\circ\text{C}; \text{ parameter: } V_{GS}$

Typ. drain-source on-state resistance

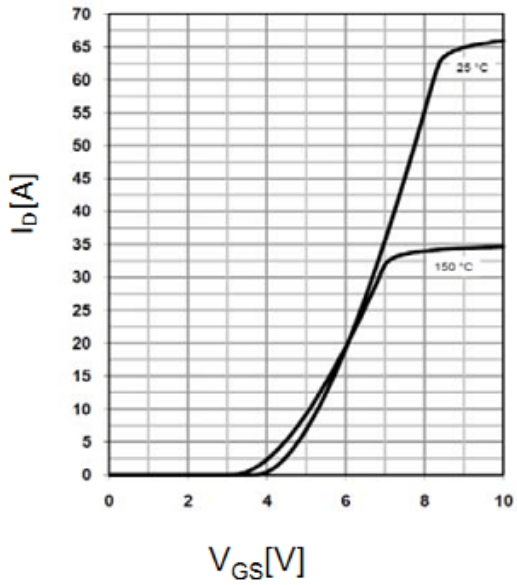


$R_{DS(on)}=f(I_D); T_j=125\text{ }^\circ\text{C}; \text{ parameter: } V_{GS}$



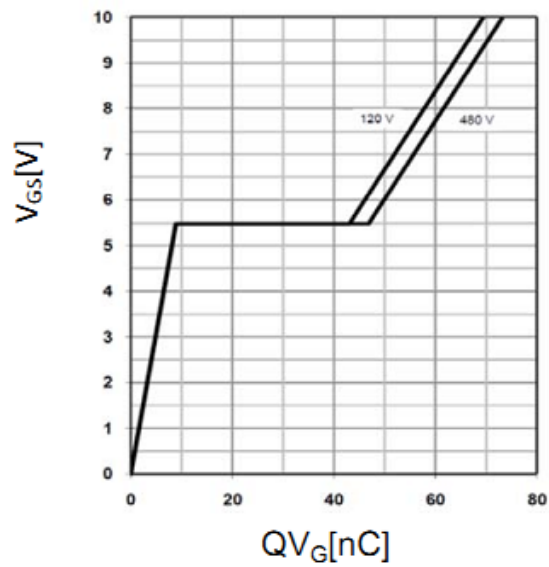
$R_{DS(on)}=f(T_j); I_D=7.3\text{ A}; V_{GS}=10\text{ V}$

Typ. transfer characteristics



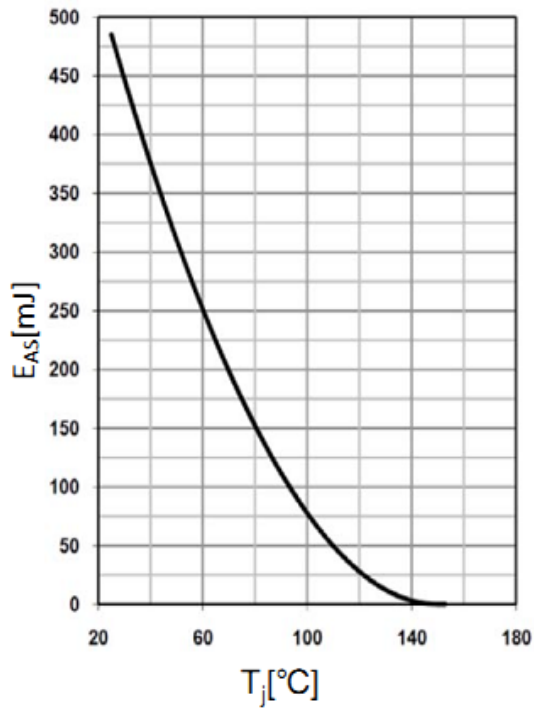
$I_D = f(V_{GS}); V_{DS} = 20V$

Typ. gate charge



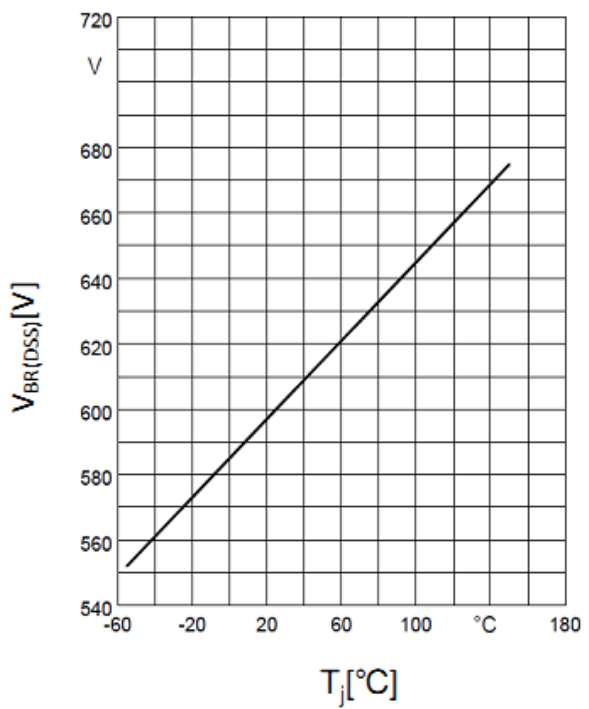
$V_{GS} = f(Q_g), I_D = 11 A \text{ pulsed}$

Avalanche energy

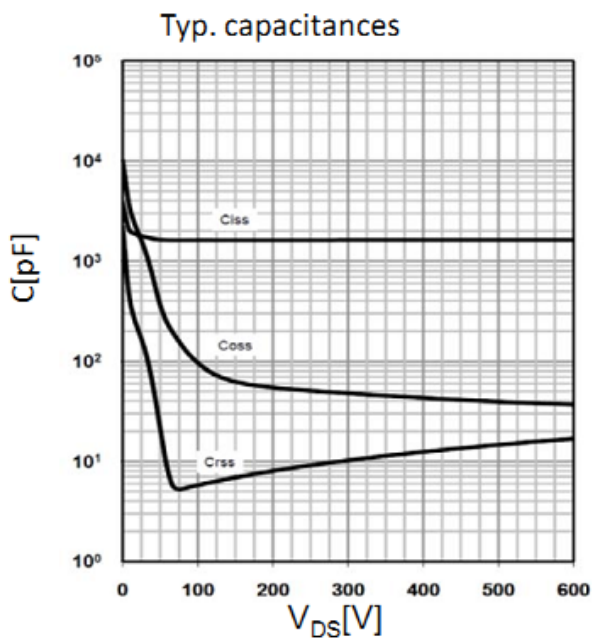


$E_{AS} = f(T_j); I_D = 3.5 A; V_{DD} = 50 V$

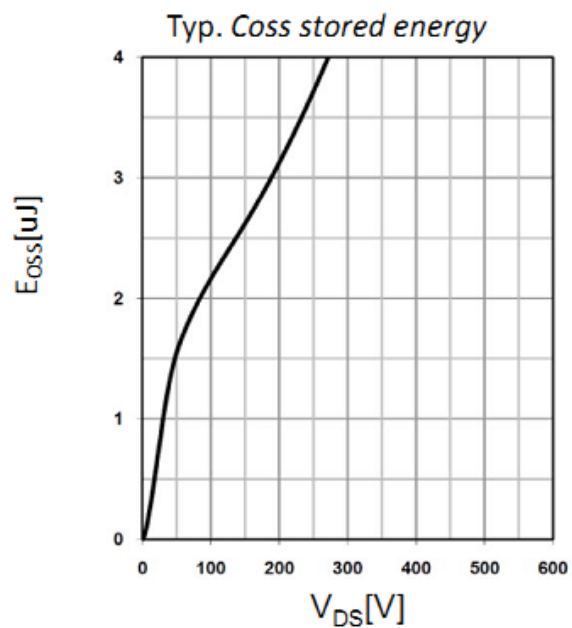
Drain-source breakdown voltage



$V_{BR(DSS)} = f(T_j); I_D = 1.0 mA$

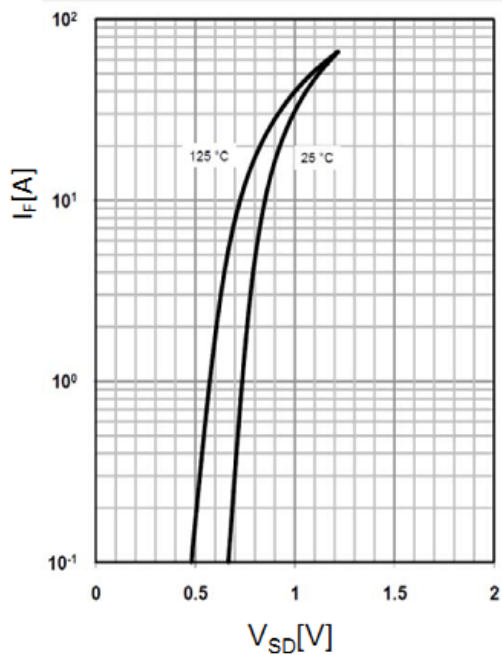


$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



$E_{OSS}=f(V_{DS})$

Forward characteristics of reverse diode

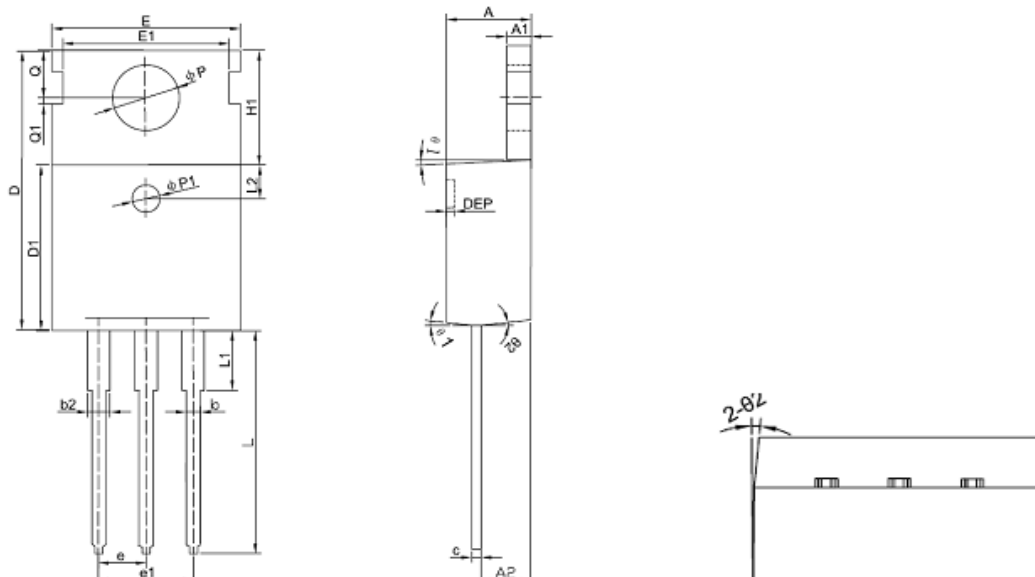


$I_F=f(V_{SD}); \text{parameter: } T_j$

SE18NS60

Package Outline Dimension

TO-220



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.590	2.690	2.790	0.102	0.106	0.110
b	0.770	-	0.900	0.030	-	0.035
b2	1.230	-	1.360	0.048	-	0.054
c	0.480	0.500	0.520	0.019	0.020	0.020
D	15.100	15.400	15.700	-	0.606	-
D1	9.000	9.100	9.200	0.354	0.358	0.362
DEP	0.050	0.285	0.520	0.002	0.011	0.020
E	10.060	10.160	10.260	0.396	0.400	0.404
E1	-	8.700	-	-	0.343	-
ΦP1	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.100	6.300	6.500	0.240	0.248	0.256
L	12.750	12.960	13.170	0.502	0.510	0.519
L1	-	-	3.950	-	-	0.156
L2	1.85REF			0.073REF		
ΦP	3.570	3.600	3.630	0.141	0.142	0.143
Q	2.730	2.800	2.870	0.107	0.110	0.113
Q1	-	0.200	-	-	0.008	-
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°

The SINO-IC logo is a registered trademark of ShangHai Sino-IC Microelectronics Co., Ltd.

© 2005 SINO-IC - Printed in China - All rights reserved.

SHANGHAI SINO-IC MICROELECTRONICS CO., LTD

Add: Building 3, Room 3401-03, No.200 Zhangheng Road,
ZhangJiang Hi-Tech Park, Pudong, Shanghai 201203, China

Phone: +86-21-33932402 33932403

33932405 33933508 33933608

Fax: +86-21-33932401

Email: webmaster@sino-ic.com

Website: <http://www.sino-ic.com>